A Low-Power Ka-band Direct Conversion Receiver Employing Half-Frequency Local Oscillator in 65nm CMOS

M.Sosio#1, A.Mazzanti*2, M.RepossiX3, F.Svelto#4

# Dipartimento di Elettronica, Università di Pavia, Via Ferrata 1, 27100 Pavia (PV), Italy
1marco.sosio@unipv.it
# Dipartimento di Ingegneria dell’Informazione, Università di Modena e Reggio Emilia
Via Vignolese 905, 41100 Modena (MO), Italy
2mazzanti.andrea@unimore.it
X STMicroelectronics - Pavia
Via Ferrata, 27100 Pavia (PV), Italy
3matteo.repossi@st.com

4francesco.svelto@unipv.it

Abstract—Direct conversion to DC by means of quadrature SubHarmonic mixers is a promising solution to arrive at low power silicon receivers working at millimeter waves. A lower frequency local oscillator (LO) does not compromise receiver performances while takes advantage of the higher quality of tuning elements and avoids high frequency, power-hungry dividers in the synthesizer. This paper summarizes our recent research efforts to arrive at a low power receiver architecture tailored to Ka band operation. The receiver IC, implemented in a 65nm CMOS technology, displays 31.5dB gain and 6.7dB NF. The LO has an outstanding frequency tuning range of 26.5% with -110dBc/Hz phase noise at 1MHz offset. Total power dissipation is 78mW only.

I. INTRODUCTION

An intense research activity toward the realization of highly integrated transceivers in CMOS operating at K band and above, in the millimetre-wave band, is currently under-way, after the Federal Communications Committee has granted unlicensed bands around 24GHz, 60GHz and 77GHz for several wireless applications [1]-[4].

The effort is presently toward compact and very low power solutions in view of integrating several transceivers on the same chip to enable phased array and smart antenna systems. To this regard, choice of the optimum front-end architecture is a key factor and mandates several peculiar considerations. A conventional direct conversion architecture, usually pursued at RF frequency, facilitates a high level of integration, eliminating image-reject and IF filters. On the other hand, synthesizing a quadrature Local Oscillator (LO) at Ka and mm-wave bands is troublesome: variable capacitors, used as tuning elements in voltage controlled oscillators (VCOs), present poor quality factors and limited component tuning, and dividers used in the PLL are power hungry. Moreover also DC offsets and inter-modulation products, due to leakage of the LO into the RF path (and reverse), are expected to increase at mm-wave frequencies due to poorer isolation between building blocks.

This paper summarizes our recent research efforts to arrive at a direct conversion receiver which mitigates the above issues by means of sub-harmonic quadrature mixers driven by a half-frequency LO [4][5]. We present a fully integrated 24GHz receiver, in 65nm CMOS, comprising a two stage LNA, a current-mode Sub-Harmonic passive mixer with a base-band trans-impedance amplifier and a 12GHz 4 phase oscillator, as shown in figure 1. Adoption of SubHarmonic mixers not only facilitates the design of the LO generation circuits but also adds benefits to the overall system performances minimizing the re-irradiated LO at the input, a primary issue in radar systems, and DC-offset induced by LO leakage. Despite the need for 4 phase generation, the proposed Local Oscillator outperforms published I & Q generators for direct down-conversion from 24GHz and it is comparable with single-phase differential oscillators. This paper is organized as follows: Section II reviews the operation principle of SubHarmonic mixers and presents the design of...
the RF front-end. Section III addresses the design of the half-frequency multi-phase Local Oscillator while measurements results are presented in section IV. Conclusions are drawn in section V.

II. RECEIVER FRONT-END

A. Multi-Phase quadrature SubHarmonic mixing

The principle of operation of SubHarmonic mixers, working with a half frequency local oscillator, is multiplication of the RF input signal times a $\pi/2$ phase shifted replica of the same square-wave reference, as shown in fig. 2a [6]. In fact, multiplication by two square-wave LOs, $\pi/2$ phase apart, corresponds to multiplication by one single square-wave reference at twice the frequency, as shown in figure 2b. The input signal at frequency $\omega_{in}$ is then down-converted at $\omega_{in}-2\omega_{ref}$ with a reference signal at $\omega_{ref}$.

For direct conversion to DC, both in-phase (I) and quadrature (Q) down-conversion paths must be implemented. It can be easily proven that I and Q down-conversion can be performed by means of a pair of half-harmonic mixers, as shown in the block diagram in fig. 1, provided the LO signals driving the quadrature path are $\pi/4$ shifted. A phase error from $\pi/4$ determines a phase departure from $\pi/2$ between quadrature down-converted signals. Applications of interest at mm-wave require relatively relaxed base-band quadrature accuracy [2][3], making the proposed architecture attractive.

B. Mixers and Base Band Amplifiers

A simplified schematic of the CMOS half-harmonic quadrature demodulator is shown in fig. 3.

The mixers core is made of two cascaded double balanced differential pairs, driven by $\pi/2$ phase shifted LO signals. For low voltage operation, the mixer is passive i.e. mosfets do not carry static current and are operated as switches. For better I&Q matching, the same High Frequency (HF) current feeds both I & Q demodulators. A differential pair, AC coupled to the mixers, is used to drive the switching core. Furthermore, being the Low Noise Amplifier single ended, the transconductor also performs single ended to differential conversion. The quadrature path, not represented for better readability, is identical to the in-phase path. A trans-impedance amplifier collects the output low frequency current. For minimum power consumption and wide bandwidth ($\approx 1$GHz), it is implemented with common-gate devices (Mc) loaded by an active current mirror (M1-2). Due to the high operation frequency, a low impedance ($1/gm_c$) loading the mixers is preferred over the high impedance alternative.

C. Low Noise Amplifier

The schematic of the LNA is shown in fig. 4 where biasing networks are omitted for simplicity. Two gain stages, in order to suppress noise of the cascaded processing blocks, e.g. mixers and base-band, have been adopted. The input stage is inductively degenerated providing 50$\Omega$ resistive impedance, at the gate of M1, for input matching. The input I network, implemented by C1,C2 and Lg, cancels out the reactive part of the input impedance. C1 and C2 also absorb the spiral and input pad parasitic capacitances versus the substrate. Output spiral inductors, L1 and L2, resonate out device parasitics for maximum gain at received frequency. To accommodate large input signals the second stage implements a variable gain feature by means of a variable resistor degenerating the input device M2, which is implemented by M3 biased in the deep triode region. Both stages make use of cascode devices, Mc1 and Mc2, to increase gain and improve reverse isolation. Due to the high frequency of operation and the single ended topology, parasitics on current return paths are extremely critical and may severely compromise performances, if overlooked. Silicon transmission lines, with
the advantage of supporting Transverse Electro-Magnetic (TEM) modes thus forward and return signal paths, can be employed to circumvent this problem. We opted for lumped element reactive components in order to save silicon area. Extensive electromagnetic simulations of the physical design have been performed to estimate parasitics since available cad tools for post-layout simulations do not prove sufficient accuracy.

III. MULTI-PHASE LO GENERATION

A ring oscillator is chosen to generate the required 4 LO phases. In order to achieve low phase noise and high-operation frequency, delay cells have been implemented with LC resonators [5]. The required sequence of four differential signals, with $\pi/4$ relative phase delay, is generated coupling four LC VCOs, as shown in figure 5. According to Barkhausen criterion, the ring assures permanent oscillation provided the loop gain is equal to 1 and the phase delay between two consecutive oscillators ($\theta$) satisfies the relation $4\theta + \pi = 2n\pi$. This equation has four different solutions in the interval $0 < \theta < 2\pi$:

$$\theta = \pm \frac{\pi}{4} \quad \text{and} \quad \theta = \pm \frac{3\pi}{4} \quad (1)$$

The four possible oscillation frequencies are symmetrically located with respect to $\omega_0$. The oscillation frequencies of the two modes corresponding to $\theta = \pm 3\pi/4$ are more away from tank resonance than those corresponding to $\theta = \pm \pi/4$. Due to a lower impedance magnitude, resulting in less loop gain, these two modes are naturally overwhelmed. Resistors $R_s$, in series with the coupling pair of figure 5b, are purposely added for discrimination of modes with $\theta = \pm \pi/4$. It can be proven that the phase shift, introduced by $R_s$ and $C_{gs}$ of transistors $M_{CP}$, provides a higher loop gain at the frequency of mode with $\theta = +\pi/4$ than for $\theta = -\pi/4$ [5]. Coupling strength between oscillators ($m=I_{CP}/I_{SW}$) is a key design parameter. Increasing $m$ degrades phase noise performance (with respect to a stand-alone oscillator dissipating the same power). To gain insight, spot phase noise simulations at 1MHz offset from the carrier versus $m$ are shown in the top plot in figure 6. To select the optimum coupling, the robustness of the relative phase shift between consecutive waveforms must be taken into account. Component mismatches and parasitic coupling between resonators cause deviation from nominal LO phase shifts. A larger $m$ reduces the phase deviation. To gain insight, we assumed a 0.5% mismatch randomly distributed among the tank capacitors. The simulated average phase error between I&Q down converted signals in a quadrature receiver based on SubHarmonic mixers driven by the multi-phase oscillator is shown in the bottom plot of fig. 6. In this framework quadrature accuracy is of minor concern [2][3] being a I&Q phase error as large as 5° tolerable. Targeting a phase error of 2° for sufficient margin, simulations indicate a required $m$ of 1 (i.e. $I_{CP}=I_{SW}$) for the 4-phase oscillator. Interestingly, not only a sub-harmonic receiver allows the adoption of a half-frequency oscillator, beneficial by itself because of the higher quality factor of passive components, but also the proposed topology for the 4-phase oscillator allows a negligible phase noise degradation ($\approx1\text{dB}$) if compared to a single phase oscillator.

The resonators are made of a center-tapped single-turn inductor of 400pH, an array of two binary weighted switched capacitors for coarse frequency tuning and thick oxide mosvaractors with $L_{g}=0.25\mu m$ for fine tuning. The control voltage ranges from 0 to 2V. The tank quality factor is 8, equally determined by inductors and capacitors. Thanks to the lower operation frequency the VCO drives directly the switching devices of the SubHarmonic mixers of figure 3, therefore avoiding the use of additional power hungry LO buffers. A frequency divider by 8, implemented with the cascade of 3 scaled divide-by-two Current-Mode Logic (CML) flip flops has been also designed to lock the oscillator to an external reference.

![Fig. 5 Block diagram of a 4-phase LC ring oscillator(a). Schematic of a delay cell (b).](image)

![Fig. 6 Simulated Phase Noise at 1MHz offset from the carrier (top) and phase error due to 0.5% tank mismatches (bottom) in the 4-phase oscillator.](image)
IV. EXPERIMENTAL RESULTS

The receiver front-end has been implemented in a 65nm CMOS technology provided by STMicroelectronics. A die photograph of the test chip is shown in figure 7.

Each building block, LO, mixers, LNA has been also implemented and tested separately. Good agreement between experimental results and simulations was found. The multi-phase VCO and divider by 8 dissipate 15mW and 8mW respectively. The frequency tuning range is 26.5% covered in 4 overlapping bands. A plot of the phase noise spectral density after the frequency divider by 8 is shown in figure 8. The equivalent phase noise at 1MHz offset from the 12GHz carrier is estimated to be -110dBc/Hz. Performances of the VCO are much better than reported quadrature LO generators at Ka band while are comparable to single phase differential VCOs.

The complete receiver has been tested with the die bonded on a PCB, low frequency signals connected with bond-wires while the RF signal was supplied by high frequency probes. Receiver conversion gain, noise figure (NF) and input matching (S11) of the LNA are shown in fig. 9. Maximum conversion gain is 31.5dB with a corresponding NF of 6.7dB. Input 1dB compression and IP3 are -24 and -13dBm respectively. As expected the leakage of the local oscillator at the input pad is extremely low: -65dBm and -90dBm at 12 and 24GHz respectively. Deviation from quadrature of the I&Q downconverted signals is better than 3°. Total power dissipation is 78mW of which 27% for the LNA, 43% for the mixers and base-band and only 30% for the LO generation.

V. CONCLUSIONS

Choice of the best receiver architecture for silicon applications at millimeter wave is key to enable high performance, low-power solutions. In this frame-work, a direct conversion architecture built around quadrature SubHarmonic mixers has the remarkable advantage of requiring a LO running at half the nominal frequency. The requirement of multiple LO phases does not compromise performances while running at half frequency saves a significant amount of power. A receiver prototype, implemented in 65nm CMOS displays state of art performances with 78mW dissipation, to the Authors knowledge, the lowest reported to date.

ACKNOWLEDGMENT

This work has been supported by an Italian research project F.I.R.B. ( # RBA06L4S5). Authors are grateful to STMicroelectronics for silicon access.

REFERENCES