On-Chip Sine Wave Frequency Multiplier for 40-GHz Signal Generator

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Abstract – This paper presents a novel signal frequency multiplier for very high speed applications. The proposed circuit is based on a simple but effective folding cell and it is able to generate an output at four times the frequency of the differential sine wave input. The circuit has been designed and optimized for a 40-nm CMOS technology and it has been fully simulated at the transistor level. Possible fabrication and timing mismatches are corrected with foreground calibration. Simulation results shows that the multiplier can provide an output signal at 40 GHz starting from a 10-GHz input signal consuming about 5 mW.

I. INTRODUCTION

With the significant growth of digital communication applications, computer networks and interfaces between the electrical and optical domain in optical networks, high-speed, and possibly low power data processing communication systems are needed. These requirements make the on-chip multi-giga clock multiplier a research area very active and in continuous evolution.

Various methods of making clock multipliers directly on-chips have been presented in the open literature. These conventional approaches use phase locked loops (PLLs) or delay-locked loops (DLLs), [1-3], which have the advantage of correcting the clock phase error in the circuit by itself. PLL-based clock multipliers, however, are known to suffer from frequency drifting and electromagnetic interference (EMI) problems. An alternative clock-multiplier approach uses a simple combinational logic and a delay line to achieve better performance at low cost, [4].

This paper proposes to use a non-linear block that obtains a folded-like input-output transfer characteristics. The non-linear response of the block transforms an input sine wave into a pseudo sine wave at double frequency. The simple scheme used to obtain the non-linear response is very fast and enables operation up to more than 40 GHz without requiring significant power consumption.

A single non-linear block multiplies by two the input frequency. By cascading two folding cells, it is possible to obtain a 4x clock multiplication, with input differential sine wave at 10 GHz and output at 40 GHz.

The circuit has been fully simulated at the transistor level with a 40-nm CMOS technology. The simulated power consumption is about 5 mW with 1-V power supply.

II. FREQUENCY MULTIPLIER

A. Use of Voltage Folding

An ideal voltage folder, as used in A/D folding architectures [5], has the input-output transfer characteristics shown in Fig. 1(a). An input sine wave with average level at the folding point is fully rectified as shown in Fig. 1(b).

Figure 1. Ideal folding transfer function (a) and output waveform (b).

Figure 2. Parabolic folding transfer function (a) and output waveform (b).

Figure 3. Gaussian folding transfer function (a) and output waveform (b).
The response is not suitable for frequency multiplication because the result contains large spur terms that must likely be removed with additional efforts. A better response is obtained with a parabolic non-linear block (Fig. 2(a)) whose response is depicted in Fig. 2(b). Another option is to have a pseudo Gaussian response (Fig. 3(a)) that also gives rise to a good frequency doubling, provided that the peak of the non-linear response is at the average level of the input and that the amplitude is proper (Fig. 3(b)).

Comparing the diagrams of Figs. 1, 2, and 3, it results that a parabolic or a Gaussian non-linear function are suitable solutions for frequency doubling.

**B. Folding Circuit**

Folding schemes, basis of this paper, that realize a static pseudo Gaussian response is shown in Fig. 4(a). They use p-channel input transistors but the use of a complementary scheme is also possible. The control is differential. When one inputs is low and the other is high, both paths are off and the output voltage is zero. At a given differential level, the paths establish conduction and the output voltage increases. When the differential input is zero, the output reaches its peak voltage. One of the schemes uses a resistive load, the other a n-channel current source. The input output response for different values of transistor sizes is shown in Fig. 4(b). Notice that the resistive load determines almost linear pieces of the response while the current source has a more rounded top.

The curve improves by the use of the draining section of Fig. 5(a) which response, given in Fig. 5(b), is more close to a Gaussian curve.

The folding circuit of Fig. 5(a) provides a single-ended output. For differential folded outputs, it is necessary to use a complementary circuit. For both versions, a proper choice of transistors sizes controls the maximum output voltage and circuit current consumption.

Monte Carlo simulations verified that transistor mismatches alter the output transfer function. The effect on multiplier performance is acceptable until a given extent and, to ensure a good yield, it is necessary to calibrate errors. Mismatch causes shift in the $V_{in}$ and $V_{out}$ directions of the transfer function. The effects are compensated for with circuit of Fig. 6 that uses the transistors $M_6$ and $M_7$, driven by the trimmed static voltages, $V_{T1}$ and $V_{T2}$. The effects of $V_{T1}$ and $V_{T2}$ are illustrated in Fig. 7. A differential component, Fig. 7(a), moves the response in the $V_{in}$ direction. A common mode signal gives the shift depicted in Fig. 7(b) in the $V_{out}$ direction. Changes of Fig. 7 require to trim $V_{diff}$ and $V_{comm}$ by only tens of mV.

The speed of the folding cell is tested with a differential step at the inputs. Fig. 8 shows the output response with a 400-mV peak to peak wave. The output voltage is an exponential with time constant of about 25 ps, corresponding to an equivalent operational frequency of 40 GHz. The limit is intrinsic of the folding cell and the used technology. Indeed, augmenting sizes of transistors to increase current also increases parasitic capacitance and the speed limit is unchanged.
C. Clock Multiplier

To obtain a 4x multiplication it is necessary to have a 2x multiplied signal and this is obtained with two complementary non-linear cells, as shown in Fig. 9.

Since outputs are not suitable to drive the input of the second multiplier, two tapered inverter chains, [6], are used at the output. The use of complementary schemes to obtain the differential outputs is source of minor mismatch in cells delay. The effect is negligible up to 5 GHz at input, but, when the frequency increases to 10 GHz, it is necessary to equalize the delay responses. This is done by the delay compensation block schematically represented in Fig. 10. Therefore, the entire 4x frequency multiplier is the cascade of two folding cells, the delay compensation and a second folding cell with output buffers.

The delay compensation block is shown in Fig. 11. It is basically composed by a CMOS inverter and binary weighted capacitors. Control bits $a_1$, ..., $a_4$ and $b_1$, ..., $b_4$ allow trimming each inverter load capacitors in the range 20 fF - 300 fF. The capacitors are made by n-MOS transistors with drain and source connected. Montecarlo simulation shows that the capacitors range allows compensating for any possible delay mismatch between n and p branches in all cases. The 4-bit trimming allows a delay accuracy of 1.5 ps, enough for a proper operation of the cascaded cell.

III. SIMULATION RESULTS

The proposed 4x clock multiplier has been simulated at the transistor level by using a 40-nm CMOS 10-metal digital technology. The supply voltage is 1 V. Input differential signal ranges from 5 to 10 GHz. The first step is the calibration of folding responses and path delay. This is assumed done at the start-up with a suitable on-board calibration network. The calibration cycle uses a slow, on-chip generated differential triangular waveform and two comparators that detect the input
levels at which folder outputs cross a desired level. The folding cell n-type uses a successive approximation calibration algorithm to match crossings of the p-type cell. The delay calibration uses test step signals and edge detectors. A search algorithm minimizes the delay between cells.

Fig. 12 shows the simulated waveforms of different nodes of the circuit depicted in Fig. 10. The inputs are 400-mV peak to peak sine waves (Vin_n and Vin_p) with common mode at half the supply voltage. The frequency is 10 GHz. The outputs are the expected signals that are almost sine waves. It can be noted that there is a delay in the responses equal to 5.5 ps. This is due to the n-folder and buffers; the p-folder with the used buffers outputs causes a delay of 3.8 ps. The use of an LSB in the delay equalizer makes almost equal the two delays providing a good pair of signals at 20 GHz for the next stage. The optimal response of the second folder, after trimming of the static response, is for a multiplied signal as small as 0.15 V. This amplitude is enhanced by the tapered buffers that bring the amplitude to the full swing as shown in the bottom diagram of Fig. 12.

The current consumption of each input folders is 1 mA. The total dynamic power consumption of tapered buffers is 1.5 mW. The power of the last folder increases to 1.5 mW because of the requests of higher speed. Therefore, the simulated total power consumption is about 5 mW.

IV. CONCLUSION

This paper proposes a new clock multiplier based on a simple but effective folding circuit. The proposed circuit achieves, without any feedback need, a multiplication by 4 of the input signal frequency by cascading two 2x clock multipliers. The multiplier uses a pseudo Gaussian folding cell whose features have been discussed. Possible mismatches and phase delay are calibrated at the start up with an on-board calibration scheme. Transistor level simulations demonstrate a proper operation with input up to 10 GHz. The 40-GHz output is a rail-to-rail signal thanks to the use of a tapered chain of inverters.

ACKNOWLEDGMENTS

The authors would like to thank FIRB, Italian National Program #RBAP06L4S5 for partial economical support.

REFERENCES


