Experimental Analysis of RESET Resistance Distribution in Phase Change Memories

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Abstract—Phase change memories (PCMs) are promising candidates for multilevel storage, thanks to the wide programming window. The multilevel approach requires good control of the programmed cell resistance. For any multilevel programming strategy, the RESET operation plays a key role for the accuracy of the intermediate programmed resistance levels. In this paper, we analyze the impact of the applied RESET pulse amplitude and the fabrication process spreads on the resistance distribution obtained after the RESET operation. To this end, we propose a model to estimate the impact of device parameter spreads on the amorphous cap thickness and, hence, on the cell resistance obtained after a RESET operation. The proposed model is verified by means of experimental characterization on a PCM cells array.

I. INTRODUCTION

Phase change memories (PCMs) have recently gained increased attention among emerging non-volatile memory technologies. A PCM cell consists of a thin layer of chalcogenide alloy ($Ge_2Sb_2Te_5$, GST), which can be reversibly switched between two structural phases having significantly different electrical resistivity: the amorphous phase (highly resistive) and the (poly)crystalline phase (less resistive). Phase transition is achieved via thermal stimulation induced by means of Joule heating: the temperature inside the material is indirectly controlled by applying a suitable electrical pulse to the cell. In bilevel applications, a PCM cell is programmed either to the full-SET state (minimum resistance) or to the full-RESET state (maximum resistance). The possibility of multilevel (ML) storage (i.e., the possibility of storing more than one bit per cell) is allowed by the large difference between the resistances of the RESET and the SET state. The ML approach in PCM devices requires accurate programming of the cell resistance to predetermined intermediate levels [1], [2]. Two alternative ML programming strategies have been proposed in the literature, namely partial-SET and partial-RESET programming. In the former case, the PCM cell is first programmed to the full-RESET state and, then, a sequence of partial-SET pulses is applied in order to partially crystallize the amorphous volume [2]. In the latter case, the PCM cell is first programmed to the full-SET state and, then, the GST material is partially amorphized by means of partial-RESET pulses [3]. In both cases, the resistance of the programmed intermediate state depends on the distribution of the amorphous and crystalline phases inside the GST layer. In particular, the thickness of the amorphous cap after the RESET operation is a key parameter to control the resistance of the intermediate states in the case of partial-RESET programming. However, the amorphous cap thickness is also important in partial-SET programming since, in this case, it affects the maximum achievable value of the cell resistance and, hence, the programming window (i.e., the resistance range wherein all programmed states must be allocated).

The thickness of the amorphous cap and, as a consequence, the RESET-state resistance, are highly sensitive to the process spreads of device parameters (in particularly, of heater, select and bias transistors). Optimized heater geometries have been proposed in the literature in order to limit the sensitivity of the programmed resistance values to fabrication process spreads [4], [5], [6]. Nevertheless, the spreads of the programmed resistance depends on the amplitude of the programming pulses, the sensitivity can also be reduced by means of effective and robust ML programming algorithms even when considering optimized cell geometries.

The aim of this paper is to analyze in detail the impact of the RESET operation over the RESET resistance spreads, in order to provide a design guideline for the choice of the optimum RESET pulse. To this end, we propose an analytical model to estimate the mean thickness and the thickness spread of amorphous cap obtained by applying a RESET pulse of a given amplitude to a cell in its full-SET state. The proposed model is validated by comparing the obtained relations with experimental results.
the experimental results.

II. CELL ARCHITECTURE AND SIMPLIFIED THERMAL MODEL

A memory cell of the considered test-vehicle [7] consists of a PCM storage element in series with two MOS selectors (Fig. 1). The storage element is composed of a top electrode contact (TEC, titanium), a thin GST stripe, a heater (titanium nitride), and a bottom electrode contact (BEC, tungsten). For the considered 180-nm technology node, the contact area between the heater and the GST is about 1600 nm², and the thickness of the GST layer is 80 nm. To develop an analytical model capable of estimating the thickness of the amorphous cap obtained after a RESET pulse, we considered the simplified cell geometry of Fig. 2(a).

The maximum temperature inside the chalcogenide layer, which is achieved at the heater-GST interface [8], can be expressed as

\[ T_{\text{max}} = R_{\text{th}} \frac{V_{\text{RST}}^2}{R_h} + T_0, \]

where \( R_h \) is the heater electrical resistance, \( V_{\text{RST}} \) is the voltage applied across the PCM cell during the RESET operation, \( T_0 \) is the thermal ground temperature, and \( R_{\text{th}} \) is the equivalent thermal resistance of the PCM device from the heater-GST interface to the thermal ground (represented by the top-electrode and the bottom-electrode contacts). Notice that \( R_{\text{th}} \) is used in Eq. (1) instead of the cell resistance since, during the RESET pulse, the resistance of the chalcogenide layer is negligible as compared to \( R_h \), due to the threshold switching phenomenon [9]. The temperature inside the GST layer decreases from its maximum value \( (T_{\text{max}}) \) to a minimum value (room temperature, \( T_0 \)) at the top electrode contact. In order to evaluate the temperature distribution inside the PCM cell, we implemented a 3D model of the cell [8] and carried out an electro-thermal simulation. The obtained temperature profile is shown in Fig. 2(b). The temperature profile inside the GST decreases almost linearly with the distance from the heater-GST interface, since the heat flow from the heater to the TEC is substantially parallel to the z-axis. Therefore, we used the simple linear model shown in Fig. 3 to calculate the distance \( x_A \) from the heater at which the temperature in the GST is equal to the melting point \( T_{\text{melt}} \), thus obtaining the following equation

\[ x_A = h \left( \frac{T_{\text{max}} - T_{\text{melt}}}{T_{\text{max}} - T_0} \right) = h \left( 1 - \frac{(T_{\text{melt}} - T_0)R_h}{R_{\text{th}}V_{\text{RST}}^2} \right), \]

where \( h \) is the thickness of the GST layer. It is worth noting that \( x_A \) does not linearly depend on \( V_{\text{RST}} \) or on the RESET programming power \( \left( \frac{V_{\text{RST}}^2}{R_h} \right) \). Furthermore, \( x_A \) asymptotically approaches \( h \) as \( V_{\text{RST}} \) tends to infinity due to the effect of the TEC, which is considered to be at room temperature. Let us define \( V_{\text{RST,min}} \) as the lowest amplitude of the RESET pulse that, applied to a PCM cell in the full-SET state, causes a significant increase of the measured resistance (in this condition, the volume of GST material close to the heater-GST interface is heated just above the melting point). The equivalent thermal resistance \( R_{\text{th}} \) can be expressed as

\[ R_{\text{th}} = \frac{(T_{\text{melt}} - T_0)R_h}{V_{\text{RST,min}}^2}, \]

and, hence, by substituting Eq. (3) in Eq. (2), we get

\[ x_A = h \cdot \left( 1 - \frac{V_{\text{RST,min}}^2}{V_{\text{RST}}^2} \right) = h \cdot f(V_{\text{RST}}), \]

where \( f(V_{\text{RST}}) = \left( 1 - \frac{V_{\text{RST,min}}^2}{V_{\text{RST}}^2} \right) \) can be seen as a thick-
ness modulation factor. The distance $x_A$ corresponds to the thickness of the amorphous cap obtained after the RESET operation. Since the resistance of the remaining (crystalline) GST can be considered to be negligible with respect to the resistance of the amorphous GST (provided that $\rho_A x_A \gg \rho_{ch}, \rho_C$ and $\rho_A$ being the low-field resistivity of the crystalline and the amorphous GST, respectively), the GST resistance is given to a good approximation by

$$R_{GST} \approx \rho_A x_A,$$

where $A$ is the contact area between the heater and the GST layer. $R_{GST}$ depends linearly on $x_A$, since the heat flow component along the $z$-axis is the dominant one inside the GST layer. Thus, the width of the amorphous cap along the $x$-axis and the $y$-axis is much larger than its thickness. By replacing Eq. (4) in Eq. (5) we obtain

$$R_{GST} \approx R_{max} \cdot f(V_{RST}),$$

where $R_{max} = \rho_{ch} x$ is the asymptotic maximum resistance which is achieved in case of a fully amorphous GST layer.

If we now consider fabrication process spreads, the relative error of $R_{GST}$ is given by

$$\frac{\Delta R_{GST}}{R_{GST}} = \sqrt{(\frac{\Delta R_{max}}{R_{max}})^2 + (\frac{\Delta f}{f})^2}.$$  

(7)

It is worth noting that the relative error of $R_{max}$ is not affected by the amplitude of the applied RESET pulse, and is mainly due to the spreads of the contact area. Its contribution to the spread of $R_{GST}$ can be estimated to be in the order of a few percents. As will be seen in the following Section, this contribution is small as compared to the relative error introduced by the modulation factor $f$ and, hence, it will be neglected in the following analysis. Eq. (8) then reduces to

$$\frac{\Delta R_{GST}}{R_{GST}} \approx \frac{\Delta f}{f}.$$  

(8)

If we now consider the deviation $\Delta V_{RST,min}$ of the minimum reset voltage $V_{RST,min}$ from the nominal value, we can obtain the relative deviation of $R_{GST}$ that turns out be given by

$$\Delta' R_{GST} = \frac{\Delta R_{GST}}{\langle R_{GST} \rangle} \approx \frac{2 \Delta V_{RST,min}}{V_{RST}^2} (\langle V_{RST, min} \rangle)^2.$$  

(9)

where $\langle R_{GST} \rangle$ and $\langle V_{RST, min} \rangle$ denote the average values of $R_{GST}$ and $V_{RST, min}$, respectively. From Eq. (9), the larger the amplitude of the RESET pulse $V_{RST}$, the lower the relative deviation of the obtained resistance. In particular, when considering two RESET pulses with different amplitudes $V_{RST,1}$ and $V_{RST,2}$, the corresponding relative deviations $\Delta' R_{GST,1}$ and $\Delta' R_{GST,2}$ are related as follows:

$$\frac{\Delta' R_{GST,1}}{\Delta' R_{GST,2}} = \frac{V_{RST,2}^2}{V_{RST,1}^2 - (\langle V_{RST, min} \rangle)^2}.$$  

(10)

### III. EXPERIMENTAL RESULTS

We carried out the experimental validation of the above model on a 4-Mb MOSFET-selected μtrench-cell PCM chip fabricated in 180-nm CMOS technology [7]. We considered a sub-array of 1024 memory cells. First, we estimated the value of the equivalent thermal resistance $R_{th}$ of the PCM cell. More specifically, we programmed the cells of the array to the full-SET state, determined the distribution of $V_{RST,min}$ over the array, and then, calculated $R_{th}$ by means of Eq. (3). From our measurements, $V_{RST,min}$ turned out to be approximately equal to 2.8 V. Since, in our case, $R_{th} \approx 5 \Omega$, $T_{melt} = 600$ °C and $T_0 = 20$ °C, the equivalent thermal resistance $R_{th}$ was calculated as about $360 \cdot 10^3 \Omega \cdot {\text{W}}$. The resistivity value of amorphous GST $\rho_A$, estimated from the measured GST resistance of cells programmed with the highest RESET pulse amplitude, turned out to be about $26 \cdot 10^{-3} \Omega \cdot {\text{m}}$.

We programmed the considered sub-array to the full-SET state, and then applied a single 100-ns RESET pulse to every cell and measured the obtained GST resistance. We repeated the above measurements with different amplitudes of the RESET pulse in the range from about 3.4 V to 4.3 V, any amplitude value being used for all the considered cells after the re-initializing full-SET pulse.

![Fig. 4](image4.png) **Fig. 4.** Mean value of the measured cell resistance after the RESET operation as a function of the RESET pulse amplitude. The standard deviation of the resistance distribution is shown in the inset.

![Fig. 5](image5.png) **Fig. 5.** Experimental and predicted values of the amorphous cap thickness as a function of the RESET pulse amplitude.
The mean value of the measured cell resistance as a function of $V_{RST}$ is plotted in Fig. 4. $R_{GST}$ increases with the amplitude of the RESET pulse, since a higher portion of GST is melted and then amorphized, thus leading to an increase in the thickness of the amorphous cap. It can be noted from the inset in Fig. 4 that the standard deviation of the resistance distribution decreases as the amplitude of the RESET pulse increases. In particular, the standard deviation of $R_{GST}$ for the minimum considered $V_{RST}$ is about 50% higher than that obtained with the highest value of $V_{RST}$.

Then, Eq. (4) was used to predict the thickness of the amorphous cap as a function of $V_{RST}$ belonging to the considered range. As shown in Fig. 5, data and model are in good agreement. Notice that the sub-linear dependence of the thickness of the amorphous cap from $V_{RST}$ is due the presence of the TEC, which behaves like a thermal ground.

Finally, for each considered RESET amplitude, we compared the normalized standard deviation of $R_{GST}$ derived from experimental data and $\Delta R_{GST}$ as given by Eq. (9). As shown in Fig. 5, very good agreement is observed also in this case.

IV. CONCLUSION

In this paper, we analyzed the RESET operation on an array of PCM cells. In particular, we focused on the impact of both the RESET pulse amplitude and the fabrication process spreads on the resistance distribution obtained after the RESET operation. We proposed a model to estimate the mean thickness of the amorphous cap and, thus the mean RESET resistance, as a function of the RESET pulse amplitude. Moreover, the model can be used to estimate the effect of fabrication process spreads on the amorphous cap thickness, showing that the relative resistance spreads decrease with increasing amplitude of the RESET pulse. The proposed model has been verified with an experimental characterization on an array of PCM cells.

V. AKNOWLEDGMENTS

This work has been supported by Italian MIUR in the frame of its National FIRB Project RBAP06L4S5.

REFERENCES