An All-Digital PLL with a First Order Noise Shaping Time-to-Digital Converter

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Abstract—This paper presents an All Digital PLL (ADPLL) based on a first order noise shaping Time-to-Digital Converter (TDC). The architectures of two state-of-art ADPLLs and a state-of-art Gated Ring Oscillator (GRO) TDC are described. The architecture of the GRO TDC is compared with that of the proposed Local Oscillator based TDC (LO TDC) in terms of spectral performance. Behavioral Verilog-AMS models of the LO, exact LO, and exact GRO TDCs are described briefly. Finally, the Verilog-AMS models of three ADPLLs, including the TDC models, are compared by means of simulations.

I. INTRODUCTION

All Digital Phase-Locked Loops (ADPLL) have emerged as an alternative to more traditional analog PLLs for fine geometry digital CMOS, with recent results demonstrating that digital frequency synthesizers with GSM level noise performance can be achieved [1]. One of the key advantages of ADPLLs over their analog counterparts is that they remove the need for large capacitors within the loop filter by utilizing digital circuits to achieve the desired filtering function. The resulting area savings are critical for achieving a low-cost solution, and the overall PLL implementation is more readily scaled down in size as new fabrication processes are utilized [2]. Also, by avoiding analog-intensive components such as charge pumps, a more attractive, mostly digital, design flow is achieved [2].

ADPLL architectures can be classified as TDC-based and accumulator-based, as shown in Figs. 1a and 1b, respectively.

The main difference between the two architectures is how the phase error between the reference and feedback signals is generated. In TDC-based ADPLLs, shown in Fig. 1a, the TDC output is proportional to the phase error. In this case, the phase error is obtained by measuring the delay between the positive (or negative) edges of the output signals from the reference oscillator and the divider.

By contrast, in accumulator-based ADPLLs, shown in Fig. 1b, the phase error is generated by means of the difference between the reference and feedback phase signals. In this case, phase accumulators generate the phase signals directly. The model of a phase accumulator is illustrated in Fig. 2. The counter counts the positive- or negative-going edges of the input signal. The sampler reads the output of the counter every period of the clock signal. If the counter were reset every period of the clock signal, the output of the sampler would be a measure of the input signal frequency, by definition. However, since the counter is never reset1, a measurement of the input signal frequency is accumulated every period of the reference signal. We recall that phase is the integral of frequency. Therefore, the output of the sampler is a measure of the phase of the input signal, by definition. In order to realize a frequency synthesizer, the reference phase signal is obtained by accumulating the value of the Frequency Command Word (FCW) [1] every positive- or negative-going edge of the input signal. FCW is equivalent to the division ratio in a standard PLL-based frequency synthesizer.

The maximum error on the phase signal is equal to one period of the clock signal. Hence, only integer-N fractional frequency synthesizers can be realized with phase accumulators. In order to reduce the error on the phase signal and to

1The counter is simply rolled over.
realize a fractional-N frequency ADPLL, an additional TDC, labeled “Fractional Error” in Fig 1b, can be used to measure the residual fractional phase error.

Finally, the re-timing block is necessary to synchronize the outputs of the two phase accumulators.

II. Noise Shaping TDC

In a TDC [3], a reference time interval \( T_{ref} \) is used to measure an unknown time interval \( t_m[n] \) by counting how many intervals of duration \( T_{ref} \) are included in \( t_m[n] \). The output of the TDC is given by:

\[
out[n] = res \cdot \text{round} \left( \frac{t_m[n]}{res} \right) = t_m[n] + e_q[n],
\]

where \( res \) is the resolution (equal to \( T_{ref} \)), \( \text{round}(\cdot) \) is the rounding function, and \( e_q[n] \) is the quantization error at step \( n \).

In a TDC based ADPLL, the phase error\(^2\) defines the time interval to be measured\(^3\). In particular, after a time interval to be measured, there is typically a time interval in which the measurement is not required and the TDC is not operating, because the value of the phase error is not associated with that interval\(^4\). Noise shaping can be used to increase the effective resolution of a TDC by including in every measurement the quantization error associated with the previous measurement [2]. The equation describing the output of a noise shaping TDC is:

\[
out[n] = res \cdot \text{round} \left( \frac{t_m[n] - e_q[n-1]}{res} \right).
\]

Therefore,

\[
out[n] = t_m[n] - e_q[n-1] + e_q[n].
\]

In the \( z \)-domain Eq. (3) can be written as:

\[
Out(z) = T_m(z) + E_q(z)(1 - z^{-1}).
\]

Equation (4) shows that the quantization error is first order noise shaped.

A first order noise shaping TDC based on a Gated Ring Oscillator (GRO) was proposed in [4]. The concept of the GRO TDC is illustrated in Fig 3. The GRO is enabled only during the measurement interval. \( T_{ref} \) is equal to the propagation delay of a CMOS inverter. The state of the GRO is retained during the time interval between two consecutive measurements. At the beginning of every measurement, the initial state of the GRO includes the quantization error of the previous measurement and consequently first order noise shaping is achieved [2].

The block diagram of the Local Oscillator-based TDC (LO TDC) is shown in Fig. 4. \( T_{ref} \) is the period of the local oscillator. Figure 5 shows the waveforms in the LO TDC. The counter counts the positive-going edges of the local oscillator. The counter is reset when the PFD output reaches 1 or -1. The counter output is sampled when the PFD output reaches zero, namely at the end of every phase error measurement. The sign block, which depends on the sign of the phase error, adds the sign bit to the output\(^5\). The local oscillator is not stopped between two consecutive time intervals. Therefore, the first reference time interval that is used to measure \( t_m[n] \) is equal to \( T_{ref} \) minus the residual fractional part of the last reference time interval used to measure \( t_m[n-1] \). Since the residual fractional part of the last reference time interval is equal to \( e_q[n-1] \) by definition, the quantization error is first order noise shaped. Note that the proposed TDC measures all of the input time intervals, even if no phase noise information is associated with them. Noise shaping is also applied to all the measured

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\(^2\)By definition, the phase error is proportional to the time delay between the edges of the reference signal and the output of the divider.

\(^3\)Each time interval is defined by two consecutive transitions of a signal.

\(^4\)For a PFD, we assume that the phase error is associated with the time intervals during which the PFD output is equal to 1 or -1. An example of a PFD output is shown in Fig. 5.

\(^5\)We assume that the phase error is positive or negative when the PFD output is equal to 1 or -1, respectively.
time intervals. However, the sampler output is updated only during the time intervals associated with the phase noise.

In the GRO TDC, the charge at the output node of every CMOS inverter is redistributed after disabling the GRO, causing unwanted switching of the inverters; extra circuitry is required to address this problem [5]. The LO TDC solves the problem of charge redistribution, since the local oscillator is never disabled. Another advantage of the LO TDC compared to the GRO TDC is that more degrees of freedom are available in the design of the LO compared to the GRO. For example, the GRO in [5] implements a multi-counter structure, namely a counter is associated with every stage of the GRO. By contrast, the LO TDC proposed in this work is based on one counter only. However, the LO TDC could be augmented with a multi-counter structure by using a ring oscillator as the LO and a counter for every stage of the LO. In a multi-counter LO TDC, the resolution is equal to the propagation delay of a single stage. By contrast, the resolution of a single-counter GRO TDC is equal to the period of the GRO. Hence, the LO and GRO TDCs exhibit the same resolution when both of them are based on single-counter or multi-counter structures.

III. VERILOG-AMS MODELS

A. TDC model

We have used an exact behavioral model of an LO TDC to validate the models developed in this work. The exact LO TDC model uses the Verilog-AMS event detection function [6] to evaluate the exact values of the time intervals to measure. Then, Eq. (3) is used to generate the output of the Verilog-AMS model. Therefore, the exact TDC is an ideal implementation of the first order noise shaping equations. Moreover, in order to reproduce the behavior of the LO TDC, all the time intervals are measured and first order noise shaping is applied to every measurement. However, the output of the reference TDC is updated only with the measured values associated with the time intervals of the phase error. By contrast, the Verilog-AMS model of the LO TDC includes behavioral models of the local oscillator, the phase detector, the counter, the sampler, and the sign block. The exact model of a GRO TDC is implemented by using almost the same code as for the reference TDC model. However, the ideal GRO TDC measures only the time intervals associated with the phase noise.

B. ADPLL model

The block diagram of an ADPLL using our LO TDC is illustrated in Fig. 6. In the ADPLL, the digital filter is modeled by means of event detection functions and finite difference equations. The clock of the digital filter is the output signal of the reference oscillator. We designed the ADPLL with the phase margin and settling time\(^6\) equal to 60° and 200 \(\mu\)s, respectively. The z-domain equivalent transfer function chosen to implement the digital filter is:

\[
H(z) = \frac{\omega_p (z + \frac{\omega_p}{f_s} - 1)}{f_s (z - 1) (z + \frac{\omega_z}{f_s} - 1)}.
\]

where \(f_s\) is the sampling frequency (equal to the frequency of the reference oscillator), \(\omega_p = 243\) rad/s and \(\omega_z = 34\) rad/s.

A frequency divider is included in the DCO in order to speed up the simulation by avoiding the generation of a high frequency output signal [7]. The equation describing the DCO is:

\[
F_{\text{out}} = F_{\text{in}} \cdot DCO_{\text{in}} + F_0,
\]

where \(DCO_{\text{in}}\) is the DCO input value\(^7\), \(F_{\text{out}}\) is the DCO output frequency, \(K_v = 100\) MHz/V is the slope of the DCO tuning curve at the operating point, and \(F_0\) is the free-running frequency. The DCO output signal is generated by means of the timer event generator function [6]. The input reference frequency of the ADPLL and the gain of the DCO are 1 MHz and 0.2502, respectively. All of the models could be augmented with time domain noise sources in order to predict the output phase noise of the overall ADPLL. However, no noise sources have been included in the results presented in this work.

IV. SIMULATION RESULTS

Cadence Verilog-AMS tools have been used for all the simulations presented in this section. All the results refer to transient simulations.

A. Exact LO, exact GRO, and LO TDCs

The output power spectral density of the LO TDC is compared to the output power spectral densities of the exact LO and exact GRO TDCs when the same pair of inputs is applied. One input is the output signal of a reference oscillator with a frequency equal to 100 MHz. The other input is equal to the first input signal with positive- and negative-going edges delayed by \(\Delta t\). In order to highlight the noise-shaping effect in the output signal, the value of \(\Delta t\) is a random variable with a white spectrum and uniform distribution in the range \([\Delta t_{\text{min}}, \Delta t_{\text{max}}]\).

\(^6\)In this paper, we define the settling time as the time elapsed from the instantaneous step variation of \(N\) to the time at which the ADPLL output enters and remains within \(\pm 0.003\%\) of the final value.

\(^7\)For simplicity, \(DCO_{\text{in}}\) is a voltage in the DCO model.
The spectral density of the output of the exact GRO is defined by:

$$\text{psd}_{\text{GRO}}(f) = \text{var}_{t_m} + \frac{\text{res}^2}{3} \sin^2 \left( \frac{\pi f}{f_s} \right),$$

where $\text{var}_{t_m}$ is the variance of the series of time intervals to measure, and $\text{res}$ and $f_s$ are the resolution and sampling frequency of the exact GRO TDC, respectively [8].

The LO TDC spectrum is close to the predicted spectrum, as shown in Fig. 7.

**B. Exact LO, exact GRO, and LO ADPLLs**

Figure 8 shows the transient response of the output frequency of the exact LO, exact GRO, and exact LO ADPLLS when the resolution is 10 ns and the division ratio is changed from 2402 to 2410. As can be seen, there is almost perfect agreement between the exact LO and LO ADPLL models. The local minima and maxima of the transient response of the ADPLLs show the effects of quantization in the TDC.

When $\text{res} = 10$ ns, the execution times of the simulations are 3.3 s and 239.4 s for the ADPLLs with the models of exact LO and LO TDC, respectively. Thus, the simulation of the ADPLL with the exact model is 72 times faster than the ADPLL with the LO TDC model, because the generation of the Local Oscillator output signal greatly increases the number of simulation points. The execution times of the simulation of the GRO ADPLL is 3.1 s. Since the simulation outcomes for the exact LO and LO ADPLLs are coincident, it is more convenient to study the performance of the ADPLL by using the exact LO TDC model.

**V. Conclusion**

In this paper we have presented an ADPLL with a first order noise shaping Local Oscillator based Time-to-Digital Converter (LO TDC). The behavioral Verilog-AMS models of the LO TDC, exact TDC, and an exact GRO TDC are described briefly. For the example illustrated, the output power spectral density of the exact GRO TDC has higher spectral components at lower frequencies compared to the LO TDC. Simulations of ADPLLs containing exact LO and LO TDCs show good agreement between the two models. The exact LO TDC model allows fast and efficient simulations of ADPLLs including the LO TDC.

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