2D and 3D CMOS MAPS with high performance pixel-level signal processing

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A B S T R A C T

Deep N-well (DNW) MAPS have been developed in the last few years with the aim of building monolithic sensors with similar functionalities as hybrid pixels systems. These devices have been fabricated in a planar (2D) 130 nm CMOS technology. The triple-well structure available in such an ultra-deep submicron technology is exploited by using the deep N-well as the charge-collecting electrode. This paper intends to discuss the design features and measurement results of the last prototype (Apsel5T chip) recently fabricated in a 2D 130 nm CMOS technology. Recent advances in microelectronics industry have made 3D integrated circuits an option for High Energy Physics experiments. A 3D version of the Apsel5T chip has been designed in a 130 nm CMOS, two-layer, vertically integrated technology. The main features of this new 3D monolithic detector are presented in this paper.

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1. Introduction

Monolithic Active Pixel Sensors (MAPS) in CMOS technology are considered as excellent candidates to match the stringent requirements of the future high luminosity colliding machines. They are adequate in terms of material budget as the sensor and the readout electronics are integrated in the same substrate. Moreover, they can be ground down to a few tens of microns with no significant signal loss since the operating principle is based on the collection of charge diffusing in an undepleted substrate [1]. One of the main issues with CMOS MAPS is the design of a readout architecture with the capability to manage the large amount of data foreseen at the future High Energy Physics (HEP) experiments. In imaging applications the charge processing is based on a simple three NMOS transistors (3 T) readout scheme in which the voltage signal is read out by a source follower while a couple of transistors take care of resetting the pixel and connecting the source follower to a column bus. This front-end scheme lends itself to be read out in a row-by-row fashion which is not compatible with the high data throughput foreseen for the future tracking systems. In order to overcome this limitation the authors proposed a new design approach to CMOS MAPS, which are among the first monolithic sensors with pixel-level data sparsification [2]. In this new design, the deep N-well (DNW) of a triple well commercial CMOS process is used as the charge collecting electrode and is extended to cover a large fraction of the elementary cell. Several prototype chips have been fabricated with the STMicroelectronics, 130 nm triple well planar (2D) technology. They proved that the proposed approach is very promising for the realization of a thin pixel detector with similar functionalities as hybrid pixels [3]. The characterization results of the last prototype chip are presented in this paper. The groups involved in the development of DNW-MAPS are now investigating new technology options to improve the performance of monolithic sensors. Vertical integration technology (3D) offers the possibility of stacking two or more wafers, coming from different process families, one on top of the other by means of 3D integration methods [4]. A new DNW-MAPS prototype chip has been designed and submitted for fabrication in a two tier, vertically integrated, 130 nm DNW CMOS technology provided by Chartered and Tezzaron Semiconductor [5]. In this paper the main features of such a DNW monolithic pixel detector prototype are described.

2. Deep N-well CMOS monolithic active pixel sensors

Deep N-well CMOS monolithic active pixel sensors exploit the triple well option of CMOS commercial processes to implement at the pixel level a full signal processing chain (charge amplifier, shaper, discriminator and digital readout). Following this novel concept several prototypes were fabricated in the 130 nm bulk CMOS process by STMicroelectronics. They were successfully characterized with test-bench measurements and at the Proton Synchrotron facility at CERN [2,6]. The front-end electronics of the prototypes developed so far in the framework of the SLIM5 collaboration [7] includes a classical optimum signal processor for
capacitive detectors. The scaling of Apsel4D, a $32 \times 128$ DNW MAPS matrix with data driven sparsified readout, to a matrix size of about $1 \text{ cm}^2$ requires more room in the pixel cell for additional connections from the pixel digital section to the peripheral readout logic. For this reason a shaper-less front-end electronics, designed and tested in a previous prototype \cite{8–10}, has been implemented in the Apsel5T. The schematic diagram of the analog readout chain integrated in the Apsel5T chip is shown in Fig. 1. The Apsel5T chip, whose layout is shown in Fig. 2, was submitted in January 2009 and delivered in April 2009. This prototype includes two small $3 \times 3$ matrices with different layout of the sensors for charge collection measurements and an $8 \times 8$ matrix with sequential row-by-row, 8-line parallel readout. This matrix is capable of generating a trigger signal as the wired OR of all of the latch outputs. The sensor layout has also been changed to improve the detection efficiency and to reduce the parasitic capacitance. Competitive PMOS N-wells have been moved to the center of the cell and surrounded with satellite N-wells connected to the main charge collecting electrode. According to device simulations, a detection efficiency of about 98% could be achieved with a threshold setting of 400 electrons. Two different layouts have been implemented in the prototype chip. In matrix M1 the 410 $\mu$m$^2$ collecting electrode features a main body and four N-well satellites with different shapes, while in matrix M2 the 480 $\mu$m$^2$ collecting electrode consists of an N-well with annular shape. In Apsel5T chip the preamplifier NMOS input device, featuring $W/L = 22/0.25$ (whose dimensions were chosen based on criteria for optimum detection efficiency \cite{10}), is operated at a drain current $I_D = 12 \mu$A and the power dissipation is about 20 $\mu$W/pixel. The test structures in the chip equipped with a 30 fF calibration capacitance at the preamplifier input have been tested through charge injection from an external pulser. Since the charge sensitivity depends on the bias current in the feedback network, the measurements have been performed with the value which provides the maximum value of the charge sensitivity. An average charge sensitivity of about 680 mV/fC was measured. Equivalent noise charge (ENC) characterization has been performed on the structures where the preamplifier output is accessible. A mean value of about 45 and 53 electrons has been measured for the sensor of matrix M1 and M2, respectively. Charge collection properties of the sensor have been tested by means of a low power infrared laser source. The $3 \times 3$ matrices have been scanned using a 5 $\mu$m step. Figs. 3 and 4 show the charge collected by the central pixel of M1 and M2 matrices, respectively, as a function of
the laser beam position. The grayscale plots also show the layout of the sensors and the borders of the pixel. The pitch of the structure is 40 μm. The collected charge was calculated as the ratio between the amplitude of the readout channel response to the laser pulse and the charge sensitivity measured by means of charge injection through an external pulser. Fig. 3 shows a smaller area (with respect to Fig. 4) where the averaged collected charge is above 500 electrons. This is due to the smaller area, and perimeter, of the M1 sensor compared to M2 sensor. On the other hand, M1 sensor provides a smaller equivalent noise charge due to the smaller parasitic capacitance.

3. Vertically integrated deep N-well CMOS MAPS

3D vertical integration technologies are extremely attractive for the development of monolithic pixel devices. A multilayer sensor structure promises to overcome typical limitations of MAPS fabricated in a planar technology. In a 3D DNW MAPS device, for example, a layer could host sensing electrodes and analog circuits while digital electronics could be located in upper layers (see Fig. 5). In this way, most of the PMOS and their competitive N-wells are removed from the sensor layer, increasing the fill factor and therefore the detector efficiency. A multilayer structure allows also for a smaller pixel pitch and a smaller sensor capacitance, leading to a better trade-off between noise and power dissipation. Vertical integration also opens up the possibility of using different technologies for the sensor (e.g., high resistivity, detector-grade silicon) and for the readout electronics [11].

In the framework of the 3DIC Consortium [12] a vertically integrated DNW MAPS has been designed in the Chartered-Tezzaron process. The chip, now in fabrication, includes two 3 × 3 matrices for testing the readout electronics and sensor performance (named Apsel5T-3D). Apsel5T-3D represents the evolution of the last prototype DNW monolithic sensor fabricated in a planar 130 nm CMOS technology. This section describes the main design features and discusses the expected performance of the Apsel5T-3D chip. The bottom tier of the Apsel5T-3D elementary cell includes the deep N-well sensor, whose signal is processed by a charge sensitive preamplifier followed by a threshold discriminator only partially integrated in the bottom tier. The preamplifier has the same scheme as the elementary cell integrated in a planar 130 nm CMOS technology and shown in Fig. 1. The input NMOS device features a W/L = 30/0.35 and a drain current of 20 μA. Fig. 6 shows the response, obtained from circuit simulations, of the analog chain to a 800 electron charge pulse for different values of the current $I_f$ biasing the feedback current mirror. The expected charge sensitivity is close to 730 mV/fC. A value of about 35 electrons has been obtained for the equivalent noise charge at a detector capacitance of 350 fF. The threshold discriminator is based on a differential pair with PMOS active load and is followed by a common source PMOS gain stage. The area of the input differential pair and the PMOS active load is relatively large with respect to the other transistors in order to reduce the threshold dispersion as discussed in Ref. [13]. The PMOS active load and the second gain stage are integrated in the upper layer in order to reduce the area of the competitive N-wells in the sensor layer and therefore improve the charge collection efficiency. Device simulations based on Monte Carlo methods show a detection efficiency of about 99% at a threshold setting of 400 electrons [14].

![Fig. 4. Charge collected (in electrons) by the central pixel of the M2 matrix illuminated by an infrared laser as a function of the laser spot position. The figure also shows the layout of the sensor, the competitive N-wells for the PMOS transistors located at the center of the layout and the borders of the pixel.](image4.png)

![Fig. 5. Cross-sectional view of a DNW CMOS MAPS: from a planar CMOS technology to a 3D process.](image5.png)

![Fig. 6. Signal at the output of the analog readout channel as a response to a charge pulse of 800 electrons. The waveforms were obtained from circuit simulations from different values of the current $I_f$ biasing the feedback current mirror.](image6.png)
4. Conclusions

A new deep N-well monolithic active pixel sensor has been fabricated and tested in view of the realization of matrices with larger size (about 1 cm²). The detection efficiency of the sensor has been improved by a new layout. Competitive N-wells, due to the PMOS transistors, have been moved to the center of the pixel and surrounded with satellite N-wells connected to the main body of the sensor, or with an annular geometry of the sensor. Infrared laser measurements show a limited decrease of the collected charge in the area covered by the competitive N-wells. In this shaper-less scheme more room is available for private lines for communication between pixels and electronics located at the periphery of the chip. The design of a new DNW MAPS sensor prototype in a two-layer, vertical integration process has been described. This technological solution has the capability to dramatically improve the performance of the sensor in terms of functional density and charge collection efficiency. The measurement activity is suppose to start in the second half of 2010.

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References