Algorithm for Automatic Design of Maximum-Efficiency Dickson Charge Pumps

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Abstract — This paper presents an algorithm for the automatic design of Dickson charge pumps, which allows the required output voltage level and current driving capability to be achieved while maximizing power efficiency and keeping area occupation within the allowed budget. Simulated results of two charge pumps designed by using the proposed algorithm for different fabrication technologies demonstrated the effectiveness of the approach.

1 INTRODUCTION

The increasing demand for devices with low power consumption and the continuous technology scaling down push the use of lower and lower supply voltage. In many applications, such as power integrated circuits, EEPROM’s, and Flash memories, voltages higher than the power supply $V_{dd}$ are required. In a single-supply device, high voltages have to be generated on-chip by elevator circuits, which are generally based on the charge pump principle. Key targets when designing a charge pump circuit are high current driving capability, reduced area, and limited power consumption. The last requirement, which is of outmost importance especially for portable applications, calls for adequate efficiency (defined as the ratio between the power $P_{OUT}$ delivered to the output and the power $P_{IN}$ drawn from the power supply: $\eta=P_{OUT}/P_{IN}$).

This paper presents an algorithm that automatically designs a Dickson charge pump [1], providing the required output voltage level and current driving capability while maximizing power efficiency and keeping silicon area occupation within a specified value. A key feature of the proposed algorithm is technology independence, which is vital considering the continuous evolution of fabrication technology. First, a simple mathematical model of Dickson charge pump is proposed. Based on this model, the automatic design algorithm is presented. Finally, simulated efficiency results are provided.

2 MATHEMATICAL MODEL

A very popular configuration for Dickson charge pumps is shown in Fig. 1 [2], [3]. For simplicity, the case of a 4-stage pump has been illustrated: the extension to the case of $N$ stages is straightforward. Each stage includes a pass-transistor $M_i$ ($i=1$ to $N$) and a pump capacitor $C_i$, which are driven by suitable control signals. An output stage, which includes a load, or storage, capacitor $C_L$ and a diode-connected transistor, is also present.

The control waveforms allow charge packets to be transferred from one stage to the cascaded one during each clock cycle (more precisely, pump capacitors in odd and even positions are charged during the active pulses of $\phi_2$ and $\phi_4$, respectively, whereas the load capacitor is charged during the active pulses of $\phi_1$), so that the output voltage is increased at higher levels than $V_{dd}$.

To allow charge transfer between two adjacent capacitors with no voltage drop across the associated pass-transistor $M_i$, the gate of the latter is brought to an adequately high level by driving a boost capacitor $C'_i$, which is previously pre-charged through device $M'_i$. The four phases which control the pump operation have a period equal to $T$. The time interval $T_{ON}$ devoted to charge transfer in any stage is smaller than $T/2$, to guarantee an adequate non-overlapping interval $T_{nov}$ between the corresponding transfer pulse ($\phi_2$ or $\phi_4$) and the phase which drives the associated pump capacitor ($\phi_3$ or $\phi_1$, respectively). In Fig. 1, $I_{OUT}$ represents the dc current drawn by the load. In the following, the pump capacitors, the boost capacitors, the pass-transistors, the precharge devices, the pump capacitor drivers, and the boost capacitor drivers are assumed to have the same size in all stages, and are denoted as $C$, $C'$, $M$, $M'$, $DR$, and $DR'$, respectively.
From Fig. 1, an N-stage charge pump is made up of the cascade of an input stage, \(N–1\) identical central stages, and an output stage. An equivalent circuit based on this modularity can be derived, as shown in Fig. 2. In this figure, each transfer device is modelled as an ideal switch and a series resistance \(R_{\text{ON}}\) (the transfer device in the on-state is assumed to be in triode region; clock feedthrough effects are in practice very small and, hence, are neglected). Moreover, the \(i\)-th pump capacitor represents, at the same time, the equivalent resistance of the \((i+1)\)-th stage, the \((N+1)\)-th stage being the output section.

The pump output voltage can be expressed as \([1]\)

\[
V_{\text{oUT}} = V_0 - R_{\text{ac}}I_{\text{oUT}}
\]

(1)

where \(V_0 = V_{\text{dd}} - V_0 + NV_dC/(C + C)\) is the open-circuit voltage provided by the pump \((V_0\) is the voltage drop due to \(M_{N+1}\) and \(C_l\) is the overall parasitic capacitance connected to the top plate of each pump capacitor).

From the scheme in Fig. 2, it can be derived that \(R_{\text{ac}}\) is given by:

\[
R_{\text{ac}} = \frac{T}{C + C_l} \left( \frac{e^{-\tau_c/R_{\text{ac}}}}{1 - e^{-\tau_c/R_{\text{ac}}}} \right) + (N-1) \frac{T}{C + C_l} \coth \left( \frac{T_{\text{ON}}}{2\tau_c} \right) + \frac{T - T_{\text{ON}}}{C_l} \left( \frac{e^{-\tau_c/R_{\text{ac}}}}{1 - e^{-\tau_c/R_{\text{ac}}}} \right) + \frac{T}{C + C_l} + \frac{R_{\text{ON}}}{C + C_l} + \frac{T}{C + C_l} + \frac{R_{\text{ON}}}{C + C_l} + \frac{T}{C + C_l} + \frac{R_{\text{ON}}}{C + C_l} + \frac{T}{C + C_l} + \frac{R_{\text{ON}}}{C + C_l}
\]

(2)

where \(\tau_c = R_{\text{ON}}C\), \(\tau_c = \tau_c/2\), and \(\tau_d = R_{\text{ON}}(CC)/(C+C_l)\) represent the time constants of the input, the central, and the output stage, respectively, and \(R_{\text{ON}}\) is the equivalent resistance of the diode-connected transistor in the output stage. In the above equation, the second term represents the equivalent resistance of the \((N-1)\) central stages, as also provided in \([4]\), the first term represents the equivalent resistance of the input stage, and the last two terms correspond to the equivalent resistance of the output stage together with its load.

The output current provided by the charge pump flows through the equivalent output resistance of the pump, thus leading to a resistive power consumption term \(P_{\text{ac}}\) equal to:

\[
P_{\text{ac}} = R_{\text{ac}}I_{\text{oUT}}^2.
\]

(3)

The parasitic capacitances connected to the top and the bottom plate of the pump capacitors \((C_l, C_{l})\) and of the boost capacitors \((C_{l}, C_{l})\), as well as the capacitances of the phase drivers \((C_{d}, C_{d})\), give rise to a dynamic power consumption term \(P_{\text{dyn}}\), which can be expressed as

\[
P_{\text{ac}} = \frac{N V_d^2}{T} \left[ C_l + C_{l} + \alpha_1^2 + \alpha_2^2 + \alpha_3^2 + \alpha_4^2 \right] + \frac{V_d^2}{T} \left[ (N-1)C_l \alpha_1^2 + C_{l} \alpha_1^2 \right]
\]

(4)

where the reduced voltage swing of the capacitances connected to the top plates of \(C_l\) and \(C_{l}\) has been taken into account with the factors \(\alpha_i = C_l/(C_l+C_{l})\), and \(\alpha_1 = C_{l}/(C_{l}+C_{l})\), respectively. In particular, \(C_l\) includes the top plate parasitic capacitance \(\beta C_l\) \((\beta\) being a technology parameter\) of pump capacitor \(C_l\), as well as the capacitance at the gate and the drain terminal of \(M\) (due to the connection of the top plate of \(C_l\) to the gate of \(M\) and the drain of \(M_{l+1}\) and the capacitance at the source and the drain terminal of \(M\) (due to the connection of the top plate of \(C_l\) to the source of \(M_{l}\) and the drain of \(M_{l+1}\)). \(\alpha\) includes the term \(\beta C_l\) and the capacitance at the gate terminal of \(M_{l+1}\), similarly, \(\alpha\) includes the gate capacitance of \(M\) and the source capacitance of \(M\), together with the top plate parasitic capacitance of \(C_l\), \(\beta C_l\). Moreover, \(C_l\) and \(C_{l}\) are equal to \(\beta C_l\) and \(\beta C_l\), respectively, where \(\beta\) is a technology parameter, and \(C_{d}\) and \(C_{d}\) depend on the device size in the phase drivers.

Finally, short-circuit power dissipation \(P_{\text{sc}}\) due to the phase drivers is also present:

\[
P_{\text{sc}} = N(P_{\text{sc},d} + P_{\text{sc},b})
\]

(5)

where \(P_{\text{sc},d}\) (due to one pump capacitor driver) and \(P_{\text{sc},b}\) (due to one boost capacitor driver) depend on the sizes, the rise time, and the operating frequency of the drivers.

Power efficiency \(\eta\) is given by:

\[
\eta = \frac{P_{\text{sc}}}{P_{\text{sc}}} = \frac{P_{\text{sc}}}{P_{\text{sc}} + P_{\text{sc}}} = \frac{V_d I_d}{V_d I_d + P_{\text{sc}}} = \frac{V_d I_d - R_{\text{ac}} I_d}{V_d I_d + P_{\text{sc}}}
\]

(6)

From the above equation, it can be seen that, for any given value of the charge pump parameters (number of stages and, hence, open-circuit output voltage, operating frequency, and capacitor and transistor sizes), power efficiency is a function of \(I_{\text{OUT}}\) (more specifically, \(\eta\) has a maximum for an output current value included in the current range from 0 to \(V_d/R_{\text{ac}}\)). On the other hand, for any value of \(I_{\text{OUT}}\), \(\eta\) depends on the values of the charge pump parameters, and reaches a maximum for a specific set of these values. It is therefore desirable for the designer to have an
algorithm able to find the parameters that ensure the highest efficiency of the pump for the output current value required in any specific application.

3 PROPOSED ALGORITHM

The first step when developing a design algorithm for maximum-efficiency charge pumps is to derive suitable relationships between the pump parameters, so as to reduce the number of independent variables and, hence, the search space where the optimum solution has to be found. The optimum width \( W \) and channel length of all transistors, so as to save silicon load capacitance. Therefore, the independent design parameters for the charge pump design turn out to be \( C, N, T, \) and \( W \), and the algorithm will work on a four-dimension search space. Some design constraints will be set by the designer, namely \( V_{th}, \alpha', C_L, \) and \( T_{nov} \).

Based on the above model, the proposed design algorithm evaluates the performance of the pumps whose parameters belong to the four-dimension search space, selects the pumps that meet the required design targets and, then, finds the pump which provides the maximum efficiency. To limit the search space, thereby reducing computation time, the user has to specify the lower and the upper bounds of the four independent parameters (i.e., \( C_m, N_m, T_m, W_m \) and \( C_{d}, N_{d}, T_{d}, W_{d}, \) respectively), and the corresponding incremental steps (\( C_s, N_s, T_s, \) and \( W_s \)).

The developed algorithm is divided in two parts. The flowchart of the first part is depicted in Fig. 3.

First (data acquisition), the user provides the charge pump target specifications (in particular, the values of \( I_{OUT} \), of the minimum output voltage, \( V_{OUT,min} \), that the charge pump has to guarantee, and of the maximum allowed area \( A_M \)), the design constraints (i.e., the values of \( V_{dd}, T_{nov}, C_L \) and \( \alpha' \)), the technology parameters (\( L_{min}, \) oxide thickness, \( \beta_0, \beta_0' \) and unit area and perimeter junction capacitances), and the upper and lower bound for \( C, N, T, \) and \( W \).

For any value of \( C \) within the specified bounds, the algorithm calculates the component sizes (together with the corresponding parasitic elements) of all pumps having \( W \) and \( T \) within the allowed ranges, and evaluates their respective performance. The above procedure is iterated up to the minimum value of \( N \) which allows the target electrical performance \( I_{OUT}, V_{OUT,min} \) to be achieved (higher values of \( N \) are not considered, as increasing \( N \) for any given value of \( C \) leads to decreased efficiency). The parameters corresponding to the maximum-efficiency pump for any value of \( C (W_{opt}, T_{opt}, \) and \( N_{opt}) \) are then saved. Thus, when the first part of the algorithm has been completed, a set of \( P_M = (C_M - C_n)/C_s \) charge pumps is available.

The second part of the algorithm (Fig. 4) selects the optimum pump in the above obtained set. The pumps that do not meet the specified area requirement are discarded. Among the remaining pumps, the one with the highest efficiency is chosen.
The following parameters are provided by the algorithm for the optimum pump: efficiency $\eta$, area occupation $A$, clock period $T$, stage number $N$, output voltage $V_{\text{OUT}}$, ripple voltage $V_R$ (due to the current drawn by the load), pump and boost capacitor sizes $C$ and $C'$, pass, diode-connected and precharge transistor widths $W$, $W_{N+1}$ and $W'$, and phase driver transistor widths $W_n$ and $W'_n$.

4 SIMULATION RESULTS

To evaluate the performance of the proposed algorithm, implemented on a MATLAB™ platform, two different charge pumps were designed for a 0.18-µm Flash memory process (pump A) and a conventional 0.35-µm technology (pump B).

The same design constraints ($V_{dd} = 1.8$ V, $T_{nov} = 2$ ns, $C_L = 100$ pF, and $\alpha' = 0.95$) were set for both cases. Target specifications were chosen considering the basic requirements of a charge pump used to drive the bit-lines of a Flash memory array during program operation. In particular, a different program parallelism has been assumed for the two cases: 32-cell and 16-cell programming for pump A and pump B respectively, with a current consumption for each cell of about 30 µA. The minimum charge pump output voltage, $V_{\text{OUT,min}}$, required to drive the bit-lines correctly during program operation was set to 5.5 V in both cases. The target specifications were: $I_{\text{OUT}} = 1$ mA, $V_{\text{OUT,min}} = 5.5$ V, and $A_M = 80000$ µm² for pump A, and $I_{\text{OUT}} = 0.5$ mA, $V_{\text{OUT,min}} = 5.5$ V, and $A_M = 80000$ µm² for pump B.

Tab. 1 shows the component sizes obtained for the two pumps by using the proposed design algorithm (simulation time for both cases was about ten minutes on a PentiumIV™-based personal computer).

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameter</th>
<th>Value</th>
<th>Usines of measure</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$\eta$</td>
<td>31%</td>
<td>µm²</td>
</tr>
<tr>
<td></td>
<td>$A$</td>
<td>760000</td>
<td>720000</td>
</tr>
<tr>
<td></td>
<td>$N$</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T$</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$V_{\text{PP}}$</td>
<td>7.1</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td>$W$</td>
<td>60</td>
<td>65</td>
</tr>
<tr>
<td>Pump exp</td>
<td>$C'$</td>
<td>80</td>
<td>60</td>
</tr>
<tr>
<td>Boost exp</td>
<td>$C'$</td>
<td>1.25</td>
<td>5</td>
</tr>
<tr>
<td>Pass-transistor $M$</td>
<td>$W$</td>
<td>35</td>
<td>33.3</td>
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<tr>
<td></td>
<td>$W_{\text{PP}}$</td>
<td>34.5</td>
<td>38</td>
</tr>
<tr>
<td>Pass-transistor $M'$</td>
<td>$W'$</td>
<td>9.25</td>
<td>41.5</td>
</tr>
<tr>
<td>Pump exp</td>
<td>$W_e$</td>
<td>10</td>
<td>33</td>
</tr>
<tr>
<td>Boost exp</td>
<td>$W_e$</td>
<td>0.45</td>
<td>6.40</td>
</tr>
</tbody>
</table>

Tab. 1: Algorithm results for designs A and B.

A comparison between the efficiency values of the pumps obtained by simulating the circuit scheme in Fig. 1 (component sizes in Tab. 1; ELDO™ simulations; CPU time to simulate the efficiency of the optimum charge pump about 15 minutes on a Sun Microsystems™ Ultra 60 Workstation) and the corresponding equivalent circuit in Fig. 2 (MATLAB™ simulations) was then performed. The efficiency as a function of the output current was compared for both pumps (Figs. 5 and 6). An excellent agreement is observed in both cases. It is also apparent that, for both pumps, the highest efficiency is obtained at the specified output current value.

5 CONCLUSION

Based on a simple mathematical model, an algorithm for the automatic design of maximum-efficiency Dickson charge pumps was implemented. The algorithm is technology independent, which allows its use with different CMOS integration processes. A comparison between MATLAB™ and ELDO™ simulation results has been provided to validate the algorithm performance.

References