On the Design of Single-Inductor Double-Output DC-DC Buck, Boost and Buck-Boost Converters

Massimiliano Belloni, Edoardo Bonizzoni, and Franco Maloberti
Department of Electronics
University of Pavia
Via Ferrata, 1 – 27100 Pavia – ITALY
[massimiliano.belloni, edoardo.bonizzoni, franco.maloberti]@unipv.it

Abstract – Design methodologies for Single-Inductor Dual-Output (SIDO) DC-DC switching converters are presented. The suitable control of a double feedback loop enables the single inductor sharing between two outputs with low output voltages errors and limited load-regulation. The design methods to achieve SIDO converters with a wide input supply voltage range and with an overall driving capability as large as 1.4 A have been verified with simulations at the transistor level. The switching frequency can be 3 MHz or more with a small off-chip inductor.

I. INTRODUCTION

The fast market growth of multiple-voltage battery-operated portable applications such as digital cameras, PDAs, cellular phones, MP3 players, etc. demands for more and more efficient power management systems. In this area, DC-DC switching converters play a critical role in keeping long battery life while still providing stable supply voltage together with the required driving capability, [1]. Typical features of these devices are high power efficiency, low cost, and small size, [2], [3].

Often, in portable applications, the power reduction is obtained by using multiple supply voltages for different functional blocks, [4]. However, since in a system the use of one inductor per DC-DC switching converter is expensive (in terms of area and cost) and not practical, the strategy is viable only if two or more converters share the same inductor as proposed in recent implementations (single-inductor multiple-output buck converter, [5], and boost or buck converters with double output, [6], [7]).

Since the regulation of each output requires its control loop, a multiple-output system must foresee a multi-feedback loop with the request of suitable signals processing. Moreover, it is necessary to use extra power switches that must be properly driven.

This paper studies the above mentioned design issues for Single-Inductor Dual-Output (SIDO) switching converter topologies and applies the identified solutions to a study case: a two-output single-inductor buck-boost converter able to independently regulate the two output voltages. This converter has been fully implemented at the transistor level and simulated by using a conventional 0.5-µm CMOS process. Simulation results demonstrate the effectiveness of the proposed method.

II. SISO DC-DC SWITCHING REGULATORS

The four conventional Single-Inductor Single-Output (SISO) DC-DC switching regulators topologies are shown in Fig. 1.

Fig. 1(a) is the conventional buck converter architecture. During the switch M1 on-time, $T_{on,M1}$, the inductor current $I_L$ ramps-up with a positive slope $(V_{dd}-V_{out})/L$. On the contrary, during the switch M2 on-time, $T_{on,M2}$, $I_L$ ramps-down with a negative slope $-(V_{out}/L)$. Applying the small-ripple approximation and the volt-second balance to the inductor, the conversion ratio is given by $M_{buck}=(V_{out}/V_{dd})=T_{on,M1}/T=D$, where $T$ is the switching period and the duty cycle $D$ has been defined.

The boost topology is shown in Fig. 1(b). During the switch M1 on-time, $T_{on,M1}$, the inductor current $I_L$ ramps-up with a positive slope $(V_{dd}/L)$. While, during the switch M2 on-time, $T_{on,M2}$, $I_L$ ramps-down with a negative slope $(V_{dd}-V_{out})/L$. Applying the small-ripple approximation and the volt-second balance to the inductor, the conversion ratio is given by $M_{boost}=(V_{out}/V_{dd})=1/(1-D)$.

A similar study can be done for the inverting and non-inverting buck-boost architectures, shown respectively in Fig. 1(c) and Fig. 1(d).

In order to obtain N independent outputs, a straightforward approach consists in using N independent regulators. This solution leads to waste of components (since N off-chip inductors are required), and, hence, of area. Furthermore, this method will increase the overall cost of the system. The Single-Inductor Multiple-Output (SIMO) approach overcomes these drawbacks by...
consistently reducing the system area and cost. The penalty that has to be sustained is the reduction of the overall system power efficiency due to the additional load switches.

III. SIDO DC-DC BUCK CONVERTER

A DC-DC switching regulator with multiple outputs time-shares the inductor current among the different loads. Fig. 2 shows a buck converter with two outputs (SIDO buck). While a conventional SISO buck uses just a PWM control for the switches on the supply side, namely M1 and M2, the SIDO configuration foresees two additional power switches, referred to as S1 and S2, for the inductor current time-sharing.

Figure 2. DC-DC SIDO buck converter.

![Figure 2. DC-DC SIDO buck converter.](image)

Fig. 3 shows an example of the load switched currents, I1 and I2, in the cases in which T_{on,M1}<T_{on,S1} (Fig. 3(a)) and T_{on,M1}>T_{on,S1} (Fig. 3(b)) in the Continuous Conduction Mode (CCM), being T_{on,SW} the on-time of the switch SW. The inductor current I_L is the sum of the two output currents I1 and I2. A main duty cycle D and a sharing duty cycle D1 can be defined, respectively, as follows

\[ D = \frac{T_{on,M1}}{T} \]  \[ D1 = \frac{T_{on,S1}}{T} \]  

As shown in Fig. 3, even if the buck converter operates in the CCM from the inductor point of view, currents I1 and I2, delivered to the output capacitors C_{out1} and C_{out2}, respectively, are discontinuous. Indeed, during the discontinuous periods, the two output capacitors provide the current to the loads.

In the system, two control loops are, hence, foreseen. The errors of the two outputs, \( e_i = V_{set,i} - V_{out,i} \) (i = 1, 2), are the control loops inputs. Assuming a PWM control, the regulator provides two control signals. One is used to obtain the buck converter switching, while the other to divide the clock period into two slots. The control strategy for a SIDO buck in the DCM is straightforward, [8], while, for a SIDO buck in the CCM, it has been already discussed together with the compensation scheme in [9]. Its extension to the case of a SIMO buck is approached in [5].

![Figure 3. SIDO buck output branches currents (I1, I2) in the two cases D < D1 (a) and D > D1 (b).](image)

Starting from the control circuit proposed in [9], in order to better stabilize the closed loop control system and to decrease the output voltage errors, two different processors can be used in the main and into the sharing path, \( H_m(s) \) and \( H_s(s) \), respectively, as shown in Fig. 4.

Figure 3. SIDO buck output branches currents (I1, I2) in the two cases D < D1 (a) and D > D1 (b).

![Figure 4. SIDO buck control scheme.](image)

\[ H_m(s) = k_m \frac{1 + \frac{\omega_{z1}}{s}}{1 + \frac{s}{\omega_{p1}}} \]  \[ H_s(s) = k_s \frac{1 + \frac{\omega_{z2}}{s}}{1 + \frac{s}{\omega_{p2}}} \]  

With regard to the compensation strategy:

- the poles in the origin increase the DC loop gain in order to minimize the output voltages errors;
- \( \omega_{z1} \) and \( \omega_{z2} \) cancel out the output filter double-pole \( \omega_o = 1/\sqrt{LC_{outi}} \);
• \( k_m \) and \( k_s \) set the bandwidth of the main and sharing loop affecting the transient settling times.

IV. SIDO DC-DC BOOST CONVERTER

Fig. 5 shows a boost converter with two outputs. While the SIDO buck topology needs two extra load switches, the SIDO boost architecture requires only one extra load switch in order to time-share the inductor current between the two output branches.

![Figure 5. DC-DC SIDO boost converter.](image)

Fig. 6 shows an example of the main switch (M1) current, \( I_{M1} \), and the two load switches (S1, S2) currents, \( I_1 \) and \( I_2 \), in the CCM. The inductor current \( I_L \) is equal to \( I_{M1} + I_1 + I_2 \). Also for the boost configuration, (1) and (2) define the main and the sharing duty cycles \( D \) and \( D_1 \), respectively.

![Figure 6. SIDO boost main switch M1 current \((I_{M1})\) (a) and output branches currents \((I_1, I_2)\) (b).](image)

Similar considerations discussed in the above case of the SIDO buck converter lead to the proposed SIDO boost control scheme, shown in Fig. 7. Let us consider, for instance, the waveform related to the main duty \( D \) (Fig. 6(a)). An increment of \( (\varepsilon_1 + \varepsilon_2) \) means that the whole system needs more energy, so that the duty \( D \) should increase. By contrast, a decrement of \( (\varepsilon_1 + \varepsilon_2) \) means that the whole system needs less energy, then the duty \( D \) should decrease. Consider now the waveform related to the sharing duty \( D_1 \) (Fig. 6(b)). An increment of \( (\varepsilon_1 - \varepsilon_2) \) means that the first output needs more energy, so that the duty \( D_1 \) should increase. While a decrement of \( (\varepsilon_1 - \varepsilon_2) \) means that the first output needs less energy, then the duty \( D_1 \) should decrease.

The two filters, \( H_m(s) \) in the main, and \( H_s(s) \) in the sharing path, have again the same purpose as in the SIDO buck case, but, with regard to the \( H_m(s) \) filter, the different transfer function of the boost converter has to be taken into account.

![Figure 7. SIDO boost control scheme.](image)

V. SIDO DC-DC BUCK-BOOST CONVERTER

Fig. 8 shows a buck-boost converter with two outputs. Again the SIDO buck-boost architecture needs only one extra load switch with respect to its SISO counterpart in order to time-share the inductor current between the two output branches.

Fig. 9 depicts an example of the main switches (M1, M2, M3) currents, \( I_{M1} \), \( I_{M2} \), and \( I_{M3} \), and the two load switches (S1, S2) currents, \( I_1 \) and \( I_2 \), in the CCM. The inductor current \( I_L \) is equal to \( I_{M1} + I_1 + I_2 \). The main and the sharing duty cycles, \( D \) and \( D_1 \), are again expressed by (1) and (2). Similar considerations discussed in the above case of the SIDO boost converter lead to the same control scheme (Fig. 7) also for the SIDO buck-boost converter. It is worth to point out that the different transfer function of the buck-boost configuration has to be taken into account when designing the \( H_m(s) \) filter.

![Figure 8. DC-DC SIDO buck-boost converter.](image)
VI. DESIGN EXAMPLE

The proposed design methods have been validated on a two-output buck-boost design, simulated at the transistor level using a 0.5-µm CMOS technology. The design example target specifications are a total output current up to 1.4 A, a supply voltage that can range from 2.5 V to 5.5 V, a switching frequency of 3 MHz with a single 2.2-µH inductor and two 22-µF output capacitors.

Fig. 10 shows the simulation results of a load-regulation test with a supply voltage of 3.6 V. The two output voltages, $V_{out1}$ and $V_{out2}$, are set to 3.3 V. $I_{out1}$ and $I_{out2}$ have a simultaneous step-up variation from 100 mA to 650 mA and vice versa. The output voltages drops are of about 100 mV and the settling time is about 60 µs for both voltages.

Fig. 11 shows the simulation results of a load-regulation test with a supply voltage of 3.6 V. The two output voltages $V_{out1}$ and $V_{out2}$ are set to 3.3 V. $I_{out2}$ has a step-up variation from 100 mA to 650 mA and vice versa, while $I_{out1}$ is fixed at 100 mA. The $V_{out2}$ voltage drop is of about 60 mV and the settling time is about 80 µs.

In order to increase the overall power efficiency, depending on the supply voltage $V_{in}$, the converter can work also in buck mode (M3 always off) and in boost mode (M1 always on).

REFERENCES


