A Low Power Sinc^3 Filter for ΣΔ Modulators

A. Lombardi[1], E. Bonizzoni[2], P. Malcovati[1], and F. Maloberti[2]

[1] Department of Electrical Engineering, University of Pavia, via Ferrata, 1 – 27100 Pavia – ITALY
[2] Department of Electronics, University of Pavia, via Ferrata, 1 – 27100 Pavia – ITALY

[andrea.lombardi, edoardo.bonizzoni, piero.malcovati, franco.maloberti]@unipv.it

Abstract— **In recent years, continuous research efforts have been concentrating in increasing ΣΔ modulators operating frequency, while still reducing their power consumption. Indeed, when the ΣΔ modulator figure of merit (FoM) is less than 1 pJ/conversion, the decimation filter power consumption becomes a critical parameter. This paper presents a low power sinc^3 FIR filter for ΣΔ modulators. The proposed filter implements a decimation by 4, operating at 64 MHz and consumes only 0.1 pJ/sample processed. The circuit has been implemented and simulated in a 0.18-μm CMOS technology, showing an overall power consumption reduction of about 67% with respect to a conventional design. Finally, a silicon area reduction of 17% in the combinatory part of the filter can also be achieved.**

I. Introduction

The reduction in supply voltage that accompanies the aggressive scaling of feature sizes in advanced CMOS VLSI technologies makes the realization of analogue circuits increasingly problematic, mainly because of the limited available voltage range. ΣΔ modulation [1] is becoming more and more the most attractive approach for implementing high-resolution A/D converters for low voltage applications since low precision analogue building blocks can be used. Oversampled ADCs show some advantages with respect to other kinds of converters, including more relaxed requirements for component matching and for anti-aliasing filters. Furthermore, a higher resolution can be achieved together with a good compatibility with digital VLSI technologies [2]. To be more specific, in high-resolution applications, oversampled ADCs are potentially more power efficient with respect to Nyquist-rate converters, since they can be realized by using a lower number of elements and a lower complexity. Basically, a ΣΔ converter consists of a ΣΔ modulator together with a digital signal processor (DSP). In recent years, continuous research efforts have been focused on increasing ΣΔ modulators operating frequency, while still reducing their power consumption. By interposing a decimation filter between the ΣΔ modulator and the DSP, it is possible to reduce the power consumption of the latter, by decreasing its operating frequency. Indeed, when the ΣΔ modulator FoM is less than 1 pJ/conversion, the decimation filter power consumption becomes a critical parameter, since it has to be added to the ΣΔ modulator power consumption and it has to represent a small fraction of it. The need for low power decimation filters is then evident and, hence, power consumption of digital filters is nowadays an active research area.

In this paper, a low power sinc^3 FIR filter for ΣΔ modulators is presented. The proposed filter operates a decimation by 4, working at 64 MHz and consumes only 0.1 pJ/sample processed. The proposed circuit has been implemented and simulated with a 0.18-μm CMOS technology. Simulation results demonstrate the effectiveness of the approach, by showing an overall power consumption reduction of 67% with respect to a conventional design when adopting a pipeline approach. Moreover, a reduction of silicon area by 17% in the combinatory part of the filter is achieved.

II. State of Art

The transfer function of a sinc filter is

$$H(z) = \left\{ \frac{1}{N} \sum_{i=0}^{N-1} z^{-i} \right\}^M \tag{1}$$

where M is the filter order and N is the decimation factor [3], [4]. The output sample y of the filter at time n, as a function of the input samples x, can be written as

$$y(n) = \left\{ \frac{1}{N} \sum_{i=0}^{N-1} x(n-i) \right\}^M \tag{2}$$

Therefore, expanding (2) and considering that in our case it holds $N = 4$ and $M = 3$, the following expression can be obtained

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$$y(n) = x(0) + 3x(-1) + 6x(-2) + 10x(-3) + 12x(-4) +$$
$$+12x(-5) + 10x(-6) + 6x(-7) + 3x(-8) + x(-9) \quad (3)$$

where $x(-i)$ (i = 0, 1, …, 9) represents the input value sampled i clock cycles before n.

A conventional approach to design such a filter consists in designing separately the sequential and the combinatory parts of the circuit. The first one has to store each input value for 9 clock cycles while the latter has to properly combine the input data. A more effective way to design the combinatory part of the filter consists in exploiting the symmetry of the coefficients. Indeed, (2) can be rewritten as follows

$$y(n) = x(0) + x(-9) + x(-1) + x(-8) + 2x(-1) + 2x(-8) +$$
$$+2x(-2) + 2x(-7) + 4x(-2) + 4x(-7) + 8x(-3) + 8x(-6) +$$
$$+2x(-3) + 2x(-6) + 8x(-4) + 8x(-5) + 4x(-4) + 4x(-5) \quad (4)$$

By considering the above approach, an automatic design of such a filter has been achieved by using Synopsys™. A block diagram of the obtained circuit is shown in Fig. 1.

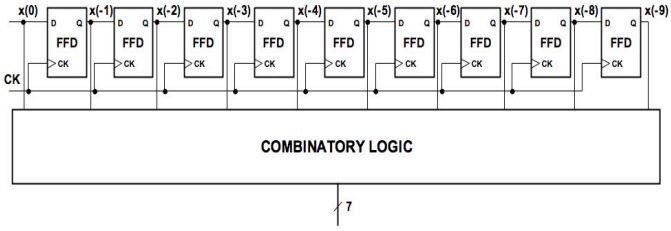

Figure 1. A sinc^3 conventional design.

The delay line (referred to as DLFF) is implemented with 9 *D*-flip-flops, which store the input values, and some standard cells used to elaborate them (block referred to as *COMBINATORY LOGIC* in Fig. 1). The power consumption and performance of the filter has been simulated by using a 0.18-µm CMOS technology. The period of the input signal is T = 15.625 ns. The delay line operating frequency is, hence, 64 MHz, while the combinatory part works at 16 MHz, taking into account the decimation filter factor, which has been chosen equal to 4. Considering a power supply equal to 1.2 V, the power consumption of the combinatory part of the system is 6.89 µW, while the sequential part of the system in simulation consumes 13.49 µW. It has to be underlined that the power consumption obtained for the sequential part is around twice with respect to the combinatory one. In this respect, a first effort in order to reduce the overall power consumption consists in implementing the sequential part of the system by using a delay line, realized in a cascade of delay cells (Fig. 2). Control signals (Φ_1 and Φ_2), together with their complementary signals ($\Phi_{1,n}$ and $\Phi_{2,n}$), allow the input signal flowing from node a to b and from b to c, respectively. With respect to a conventional approach (control phases with a duty-cycle equal to 50%), the adopted control signals timing (Fig. 2) allows reducing input data latency. In this way, T_{COMB} is the period portion in which the combinatory logic can elaborate the input data. This approach is particularly suited for high frequency applications.

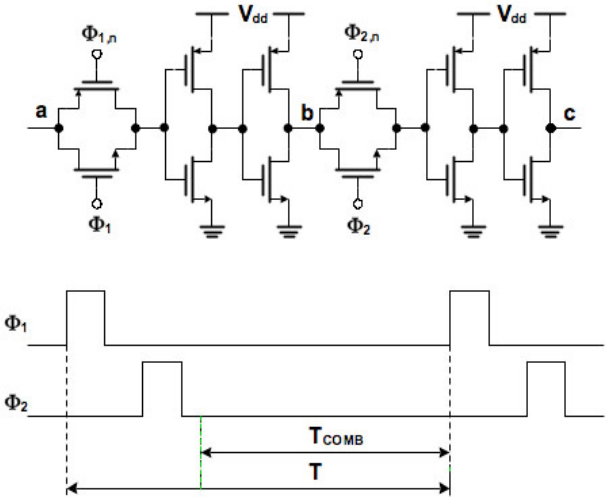

Figure 2. Delay line cell and its control signals.

The simulated delay line (referred to as DLMOS) shows a power consumption of 2.88 µW, much lower than the DLFF conventional scheme. The reduction of power consumption is by 78.6% and it is due to the overall lower transistors number (108 instead of 216) and to their smaller size. In addition, an area reduction greater than 50% can be also achieved. By referring to the whole system power consumption (i.e., considering also the combinatory power consumption), it is worth to point out that a power reduction of 52.1% has been achieved.

III. Proposed Sinc^3 Filter

The use of a plain combinatory logic, even if determined by powerful synthesis tool, is not effective when applied to specific situations. For our sinc^3 filter, we studied various alternatives to find the best low-power solution. The method followed consists in re-arranging the terms of equation (3) in blocks to obtain sub-processing systems, whose implementation can be effectively performed with minimum hardware and power consumption. In this Section, a four-step re-arrangement of (3), together with the obtained sub-systems, will be described and discussed. In particular, it can be noted that (3) can be rewritten as follows

$$y(n) = x(-0) + x(-9) + 2x(-3) + 2x(-6) + 8x(-3) +$$
$$+8x(-6) + [3x(-1) + 3x(-8)] + 2[3x(-2) + 3x(-7)] +$$
$$+4[3x(-4) + 3x(-5)] \quad (5)$$

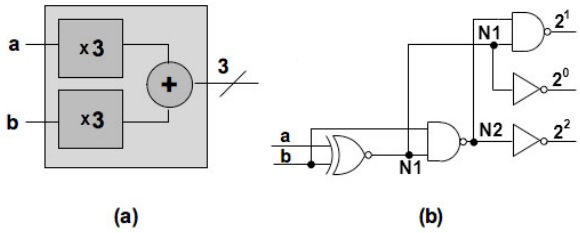

Figure 3. Cell 33: symbol (a) and circuit (b).

Expression $3a + 3b$ in (5), where a and b are two generic input bits, can be implemented by using the combinatory block, called *Cell 33*, shown in Fig. 3(a). Circuital implementation of such a block is depicted in Fig. 3(b).

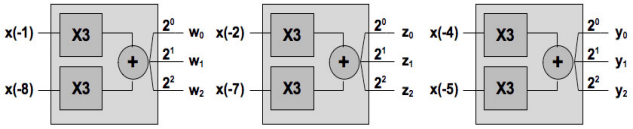

Figure 4. First step of the proposed technique.

The first step of the proposed technique consists in using the above *Cell 33* for input bits *x(-1)*, *x(-8)*, *x(-2)*, *x(-7)*, *x(-4)*, and *x(-5)*, as shown in Fig. 4. Exploiting this approach, (5) can be rewritten as follows

$$y(n) = x(0) + x(-9) + 2x(-3) + 2x(-6) + 8x(-6) + 8x(-3) + w_0 + \\ +2[w_1 + z_0] + 4[w_2 + z_1 + y_0] + 8[y_1 + z_2] + 16y_2 \quad (6)$$

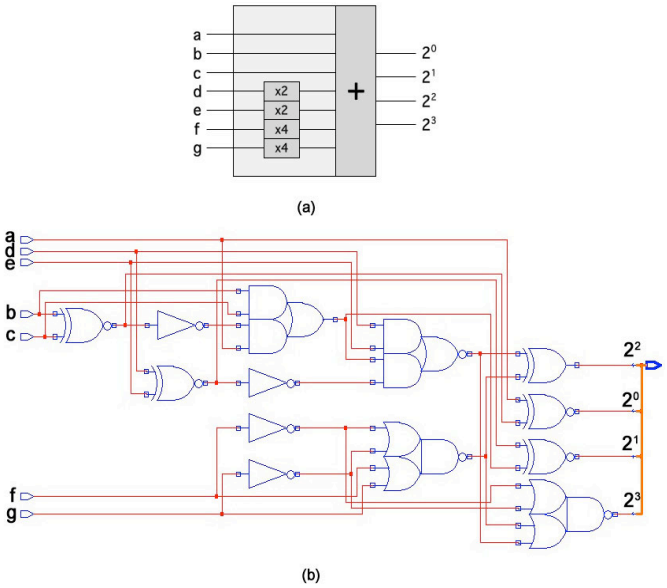

Figure 5. Cell 1112244: symbol (a) and circuit (b).

Expression $a + b + c + 2d + 2e + 4f + 4g$ in (6), where a, b, c, d, e, f, and g are generic input bits, can be implemented by using the combinatory block, called *Cell 1112244*, shown in Fig. 5(a). By using only 92 transistors, a circuital implementation of such a block can be achieved (Fig. 5(b)).

The second step of the proposed technique consists in using the above *Cell 1112244*, as shown in Fig. 6(a). Exploiting this approach, (6) can be rewritten as follows

$$y(n) = r_1 + 2r_2 + 2z_0 + 2w_1 + 4r_3 + 4z_1 + 8r_4 + 8x(-6) + \\ +8y_1 + 8z_2 + 8x(-3) + 16y_2 \quad (7)$$

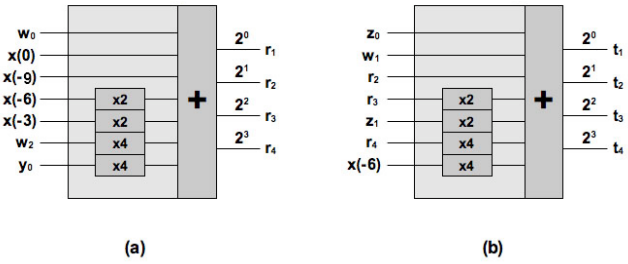

Figure 6. Second (a) and third (b) steps.

By applying *Cell 1112244* a second time (third step, Fig. 6(b)), the transfer function of a sinc^3 filter becomes

$$y(n) = r_1 + 2t_1 + 4t_2 + 8[t_3 + y_1 + z_2 + x(-3)] + 16[y_2 + t_4] \quad (8)$$

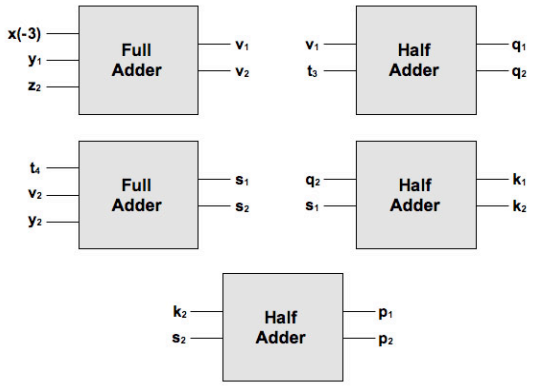

Figure 7. Fourth step.

The remaining operations are performed by means of two full-adders and two half-adders, as shown in Fig. 7 (fourth step). Parameters r_1, t_1, t_2, q_1, k_1, p_1, and p_2 represent the weighted output bits.

The proposed technique allows decreasing the power consumption of the combinatory part of the sinc^3 filter to 5.4 μW. Hence, the power saving turns out to be equal to 21.5% with respect to a conventional design. By referring to the whole system power consumption (i.e., considering also the delay line power consumption), it is worth to point out

that a power reduction of 59.4% can be achieved. Furthermore, it has to be noted that the silicon area taken by the combinatory part of the system results 17% less with respect to the conventional approach.

IV. Pipeline Approach

For the sinc^3 filter structure described in the previous Section, the main power consumption contribution is given by the commutation of MOS transistors that implies a charge or a discharge of a capacitor [3], [5]. It has to be pointed out that the main waste of power is due to the fact that often different input signals of a logic cell are stable in different instants. This results in useless commutations and, hence, in power loss. To be more specific, let us consider a very small circuit like the one depicted in Fig. 3(b). The commutation of input *b* causes, approximately in the same time, the variation of voltage at nodes *N1* and *N2*. Even if node *N2* is not stable, it forces the commutation of the two outputs 2^1 and 2^2. Then, by effect of *N1*, *N2* can change again and the related outputs too. It has to be noted that the first transition of *N2* and, hence, of the two outputs 2^1 and 2^2, is useless and increases the power consumption of the system. This concept can be applied also in each part of the filter in which non-stable signals are present.

It is worth to point out that the power consumption due to useless commutations increases with the number of transistors present in the circuit. The proposed design, made up of a block cascade connection, makes possible to split the whole circuit in different consecutive parts and, hence, to use a pipeline approach. The circuit block diagram together with the related control signals is shown in Fig. 8.

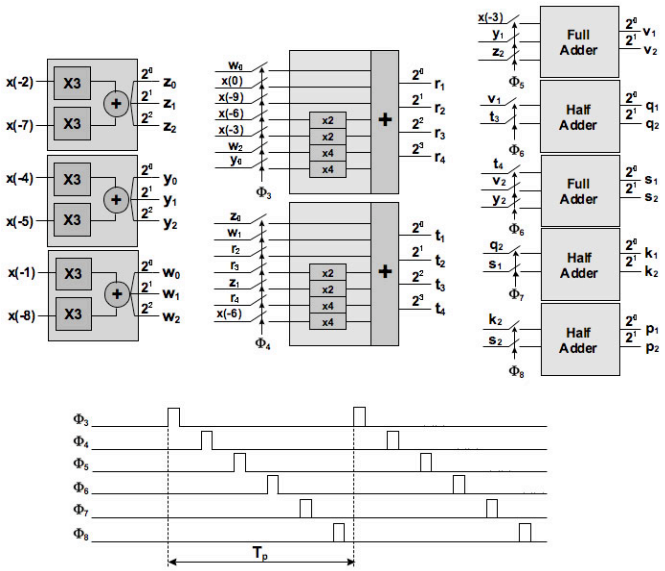

Figure 8. Proposed sinc^3 filter: pipeline approach.

When Φ_j ($j = 3, 4, \ldots, 8$) goes to its high logic level, stable inputs are presented to the related combinatory block. The period of Φ_j is $T_p = 62.5$ ns and, hence, the operating frequency is 16 MHz. By exploiting the pipeline approach, the power consumption of the combinatory part of the circuit is reduced to 3.85 μW (44% less with respect to the conventional approach) and the power consumption reduction of the whole system turns out to be 67%. It is worth to point out that to implement the pipeline approach only 66 minimum size MOS transistors have to be added and, hence, the increase in silicon area occupation can be neglected. Table 1 summarizes the simulation results.

Table 1

	Power Consumption [μW]	Power Reduction [%]
Standard Design (with DLFF)	20.38	
Standard Design (with DLMOS)	9.77	52.1
Proposed sinc^3	8.28	59.4
Pipeline sinc^3	6.73	67

V. Conclusions

In this paper, a low power sinc^3 FIR filter for ΣΔ modulators has been presented. The proposed sinc^3 filter operates a decimation by 4, working at 64 MHz and consumes 0.1 pJ/sample processed. The proposed circuit has been implemented and simulated in a 0.18-μm CMOS technology. Simulation results demonstrate the effectiveness of the approach, by showing an overall power consumption decrease of 67% with respect to a conventional design when adopting a pipeline approach. Finally, a silicon area reduction of 17% in the combinatory part of the filter can also be achieved.

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