
©20xx IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.
Hardware Reduction in Digital Delta-Sigma Modulators Via Bus-Splitting and Error Masking—Part I: Constant Input

Brian Fitzgibbon, Student Member, IEEE, Michael Peter Kennedy, Fellow, IEEE, and Franco Maloberti, Fellow, IEEE

Abstract—In this two-part paper, a design methodology for bus-splitting digital delta-sigma modulators (DDSMs) is presented. The design methodology is based on error masking and is applied to both ditherless and dithered DDSMs with constant and sinusoidal inputs. Rules for selecting the appropriate wordlengths of the constituent DDSMs are derived which ensure that the spectral performance of the bus-splitting architecture is comparable to that of the conventional design but with less hardware. Behavioral simulations and experimental results confirm the theoretical predictions. Part I addresses ditherless MASH DDSMs with constant inputs; Part II focuses on DDSMs with dither and sinusoidal inputs.

Index Terms—Bus-splitting, digital delta-sigma modulator (DDSM), dither, nesting.

I. INTRODUCTION

D I GITAL delta-sigma modulators (DDSMs) are key building blocks in a wide range of modern communication products including fractional-N frequency synthesizers, all-digital phase-locked loops (ADPLLs) and oversampling digital-to-analog converters (DACs). In a DDSM, a high resolution discrete-time input is oversampled and requantized to produce a lower resolution output. This coarse requantization takes place within a feedback loop such that the resulting quantization noise power is attenuated in the signal band of interest.

Ideally, the quantization noise introduced by the DDSM is white and uncorrelated with the DDSM’s input. In practice, however, the quantization error often forms short and repeating patterns, particularly when the input is constant, giving rise to spurious tones (spurs) in the output spectrum. Two classes of techniques have been developed to whiten the spectrum of the quantization noise: stochastic and deterministic. The primary stochastic technique is the addition of a 1-bit dither sequence to the digital input word to a high order DDSM is partitioned into a first-order DDSM was added as the input block of a third-order DDSM; this reduces the hardware complexity and produces a single-bit output. A design methodology based on error masking has been developed and applied to single-quantizer (SQ) and MASH DDSMs, reducing the hardware requirement by up to 20% without sacrificing performance [12], [13]. More recently, the authors of [14] have developed a design technique for implementing the bank of postprocessing filters in MASH DDSMs by recoding the carry output signals from the accumulators. This scheme reduces the hardware complexity of the noise cancellation network to 53% of the prior approach [15] and can be used in conjunction with error masking, which reduces the hardware complexity of the accumulators, to achieve low complexity MASH DDSMs.

In this work, we investigate a bus-splitting idea for implementing both ditherless and dithered DDSMs, in which the digital input word to a high order DDSM is partitioned into a number of parts and the LSBs are processed by one or more lower order DDSMs before being recombined with the MSBs [16]. Our work is inspired by the ideas of Norsworthy et al. [17] in which the data path of a multibit digital noise shaper is reduced by noting that noise shaping only needs to be performed on the lower few LSBs of an oversampled digital signal in order to be effective. Schreier and Temes claim that the accuracy of this scheme can be effective in terms of minimising the degradation of the SNR for sufficiently high OSR [18].

To date, the performance of bus-splitting combined with digital delta-sigma modulation has been evaluated based on insight, empirical observations, and simulations. Our goal is to formalize the method.

Manuscript received October 15, 2010; revised December 17, 2010; accepted January 12, 2011. Date of publication March 14, 2011; date of current version September 14, 2011. This work was supported in part by Science Foundation Ireland under Grant 08/IN.1/IB854, in part by the Irish Research Council for Science, Engineering & Technology (IRCSET) under the Embark Initiative, and by FIRB, Italian National Research Program, under Project RBAP06LS55. This paper was recommended by Associate Editor G. Manganaro.

B. Fitzgibbon and M. P. Kennedy are with the Department of Electrical and Electronic Engineering and Tyndall National Institute, University College Cork, Cork, Ireland (e-mail: b.fitzgibbon@umail.ucc.ie; peter.kennedy@ucc.ie).

F. Maloberti is with the Department of Electronics, University of Pavia, 27100 Pavia, Italy (e-mail: franco.maloberti@unipv.it).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSI.2011.2112890
In this paper, we provide a theoretical basis for this approach based on error masking and extend it to the case of a nested bus-splitting architecture. In Part I, we consider ditherless DDSMs with constant inputs and present design rules for selecting the word lengths of the stages to ensure that the spectral performance of the bus-splitting architecture is not degraded in comparison to the conventional design. In Part II, we consider the components that contribute to the output signal-to-noise ratio (SNR) in the case of a sinusoidal input and show how these can be manipulated to obtain a trade-off between the overall complexity of a modulator and the SNR.

This paper is organized as follows. In Section II, we review the conventional MASH DDSM architecture. In Section III, we introduce the concept of bus-splitting and review error masking. In Section IV, we explain in detail the design methodology for the bus-splitting DDSM with a constant input using the deterministic technique. We present some design examples in Section V.

II. CONVENTIONAL MASH DDSM ARCHITECTURE

Before we describe the bus-splitting architecture, we first review the conventional MASH DDSM. The basic building block of the MASH DDSM we consider in this work is the first-order error feedback modulator (EFM1) shown in Fig. 1(a). The input to the modulator is a digital word with \( N \) bits. The 1-bit quantization is achieved by taking the MSB of \( v[n] \). The discarded LSBs, representing the negative of the quantization error \( -e[n] \), are then fed back and summed with the input.

Mathematically, we can write

\[
y[n] = \begin{cases} 
0, & v[n] < 2^N, \\
1, & v[n] \geq 2^N.
\end{cases}
\]  

(1)

and the negative of the quantization error \( -e[n] \) is given by

\[
e[n] = v[n] \mod 2^N.
\]  

(2)

where \( M = 2^N \). The transfer characteristic of the 1-bit truncation quantizer is shown in Fig. 2.

An accumulator can be used to implement the EFM1 digitally, where the accumulator overflow and accumulation result correspond to the 1-bit quantizer output and the negative of the quantization error, respectively. The signal flow graph of the EFM1 is shown in Fig. 1(b), [19].

Fig. 2. Transfer characteristic of the 1-bit truncation quantizer.

In the Z-domain, we can write the output of the EFM1 \( Y(z) \) in terms of the input \( X(z) \) and the quantization error \( E(z) \) as follows:

\[
Y(z) = \frac{1}{2^N} X(z) + \frac{1}{2^N} (1 - z^{-1}) E(z).
\]  

(3)

Note that the quantization error is highpass filtered by the first-order filter \( (1 - z^{-1}) \). Higher order filtering of the quantization noise to suppress low frequency components can be achieved by using the MASH structure [20], [21].

Fig. 3 shows a block diagram of a conventional 1st order MASH DDSM comprising a cascade of \( I \) bit EFM1 blocks and a noise cancellation network. In this structure, the negative of the quantization error from each stage \( -e_i[n] \) is fed to the next stage and the output of each stage \( y_i[n] \) is fed to the noise cancellation network, which eliminates the intermediate quantization noise terms. The output of the \( I \)th order MASH DDSM can be expressed in the Z-domain as

\[
Y(z) = \frac{1}{2^N} X(z) + \frac{1}{2^N} (1 - z^{-1}) E_I(z),
\]  

(4)

where \( X(z) \) and \( E_I(z) \) are the Z-transforms of the input and the quantizer error introduced by the \( I \)th stage. Note that a conventional \( I \)th order MASH DDSM consists of \( I \) identical \( N \)-bit accumulators and a noise cancellation network. We will denote an \( I \)th order DDSM by DDSM\(_I\). In this work, we consider the MASH DDSM3, which is a popular configuration for fractional-N frequency synthesis applications [22]. The output of the MASH DDSM3 is given by

\[
Y(z) = \frac{1}{2^N} X(z) + \frac{1}{2^N} (1 - z^{-1})^3 E_3(z).
\]  

(5)

III. BUS-SPLITTING DDSM ARCHITECTURE

A. Single Split

Consider the architecture of Fig. 4, which we will refer to as a bus-splitting 1–3 DDSM3. In the case of the bus-splitting 1–3...
DDSM3, the digital input word is divided into two parts; the $N_{\text{MSB}}$ most significant bits and the $N_{\text{LSB}}$ least significant bits. The $N$-bit input can be written as

$$X = X_{\text{MSB}} \cdot 2^{N_{\text{LSB}}} + X_{\text{LSB}},$$  

where $X_{\text{MSB}}$ and $X_{\text{LSB}}$ correspond to the MSBs and LSBs, respectively, and

$$N = N_{\text{MSB}} + N_{\text{LSB}}.$$  

The output of the bus-splitting 1–3 DDSM3 can be expressed in the $Z$-domain as

$$Y_{13}(z) = \frac{X(z)}{2^N} + \frac{(1 - z^{-1})\epsilon_{Q13}(z)}{2^{N_{\text{LSB}}} \cdot 2^{N_{\text{MSB}}}} + \frac{(1 - z^{-1})^3E_{13}(z)}{2^{N_{\text{MSB}}}}$$  

where $\epsilon_{Q13}(z)$ and $E_{13}(z)$ are the $Z$-transforms of the quantization errors of DDSM1 and DDSM3 in the bus-splitting 1–3 DDSM3 architecture, respectively. Note that (8) differs qualitatively from (5) in that it contains an additional (middle) shaped noise term that results from the error introduced by the DDSM1. In particular, the output of the bus-splitting 1–3 DDSM3 contains an additional first-order shaped noise term $\epsilon_{Q13}(z)$ scaled by the factor $1/2^{N_{\text{LSB}}}$. Note that the last terms in (5) and (8) are equivalent as they represent the normalized shaped quantization error from the third-order DDSM; in particular, $\epsilon_2[n]$ is an $N$-bit word whereas $\epsilon_{13}[n]$ is an $N_{\text{MSB}}$-bit word.

By choosing the values of $N_{\text{MSB}}$ and $N_{\text{LSB}}$ appropriately, the middle term can be masked (hidden) by the shaped error term from the DDSM3 using the idea introduced in [12]. This idea is illustrated graphically in Fig. 5, where $S_1$ and $S_2$ are the spectral envelopes of the quantization noise contributions from DDSM1 and DDSM3, respectively, assuming white quantization noise. When the input is constant, the DDSM quantization noise power is spread over a number of tones that is determined by the cycle length. The first tone in $S_1$ is at $f_1 = f_s/2^{N_{\text{LSB}}}$ [12] (the details of this result can be found in Appendix A). Since $S_1$ is first-order shaped and $S_2$ is third-order shaped, all the tones of $S_1$ should be below the $S_3$ envelope if the lowest frequency tone in $S_1$ is below that of $S_3$.

### B. Nested Splitting

Consider the bus-splitting architecture of Fig. 6, which we will refer to as a nested bus-splitting 1-2-3 DDSM3. In this case, the digital input word is again divided into two parts; the $N_{\text{MSB}}$ most significant bits, and the remainder. The latter is then further subdivided into the $N_{\text{MSB}}$ intermediate bits and the $N_{\text{LSB}}$ least significant bits. The $N$-bit input can be written as

$$X = X_{\text{MSB}} \cdot 2^{N_{\text{LSB}}+N_{\text{MSB}}} + X_{\text{ESB}} \cdot 2^{N_{\text{LSB}}} + X_{\text{LSB}},$$  

where $X_{\text{MSB}}, X_{\text{ESB}},$ and $X_{\text{LSB}}$ correspond to the most significant, intermediate, and least significant bits, respectively, and

$$N = N_{\text{MSB}} + N_{\text{ESB}} + N_{\text{LSB}}.$$  

The output of the nested bus-splitting 1-2-3 DDSM3 shown in Fig. 6 can be expressed in the $Z$-domain as

$$Y_{123}(z) = \frac{X(z)}{2^N} + \frac{(1 - z^{-1})\epsilon_{Q123}(z)}{2^{N_{\text{LSB}}} \cdot 2^{N_{\text{MSB}}}} + \frac{(1 - z^{-1})^3E_{123}(z)}{2^{N_{\text{MSB}}}},$$  

where $\epsilon_{Q123}(z), \epsilon_{Q2}(z)$ and $E_{123}(z)$ are the $Z$-transforms of the quantization errors of DDSM1, DDSM2, and DDSM3 in the nested 1-2-3 architecture, respectively. Note that (11) differs qualitatively from (5) in that it contains additional shaped noise terms resulting from the errors introduced by the DDSM1 and DDSM2. Note that the last terms in (5) and (11) are equivalent as they represent the normalized shaped quantization error from the third-order DDSM; $\epsilon_3[n]$ is an $N$-bit word whereas $\epsilon_{123}[n]$ is an $N_{\text{MSB}}$-bit word.

The output of the nested bus-splitting 1-2-3 DDSM3 contains a first-order shaped noise term $\epsilon_{Q123}(z)$ scaled by the factor $1/(2^{N_{\text{LSB}}} + 2^{N_{\text{MSB}}})$ and a second-order shaped noise term $\epsilon_{Q2}(z)$ scaled by the factor $1/2^{N_{\text{MSB}}}$. By choosing the values of $N_{\text{MSB}}, N_{\text{ESB}}$ and $N_{\text{LSB}}$ appropriately, these contributions can be masked (hidden) by the shaped error term from the DDSM3. This idea is illustrated graphically in Fig. 7, where $S_1$, $S_2$, and $S_3$ are the spectral envelopes of the quantization noise contributions from DDSM1, DDSM2, and DDSM3,
and (dashed) \( S_2 \) below (solid) \( S_3 \). The lowest frequency tone in \( S_1 \) is at \( f_1 = f_s/2^{N_{MSB}} \); the lowest frequency tone in \( S_2 \) is at \( f_2 = f_s/2^{N_{LSB}+N_{MSB}} \), and \( S_3 \) are defined by (15)–(17). In this example, \( N_{LSB} = 6 \), \( N_{MSB} = 2 \), and \( N_{MSB} = 12 \).

respectively, assuming white quantization noise. The first tone in \( S_1 \) is at \( f_1 = f_s/2^{N_{MSB}} \); the lowest frequency tone in \( S_2 \) is at \( f_2 = f_s/2^{N_{LSB}+N_{MSB}} \) (details of this result can be found in Appendix A).

In the next section, we will show how to choose \( N_{MSB}, N_{LSB} \) and \( N_{MSB} \) such that the intermediate quantization terms are masked by the dominant last term.

IV. DESIGN METHODOLOGY (CONSTANT INPUT AND NO DITHER)

A. Cycle Length and Tone Location of the DDSM With Constant Input

When the input is constant, the DDSM quantization noise power is spread over a number of tones that is determined by the cycle length, resulting in a tone spacing of \( \Delta f = f_s/L_\alpha \), where \( f_s \) is the sampling frequency and \( L_\alpha \) is the cycle length [6]. The locations of these tones are given by

\[
f[k] = k \Delta f, \quad k = 1, 2, \ldots, \frac{L_\alpha}{2}
\]

where \( k \) is the index of the tone [12]. Note that in the case of an \( N \)-bit MASH DDSM3, the cycle length is \( 2^{N+1} \) when the input is odd [23].

Assuming a cycle of length \( L_\alpha \) and additive uniformly distributed white quantization noise, the idealized power spectrum of the shaped noise \( NTF(z) \cdot \epsilon_Q \) is given by

\[
S(f[k]) = \frac{1}{12L_\alpha} |NTF(z)|^2 e^{-2\pi k/\nu_L}.
\]

Throughout this paper, we will estimate the power spectrum of the actual shaped quantization noise component \( N_i \) by using the spectral envelope \( S_i \) that is obtained by assuming that the quantization noise \( E_i \) is white.

In this work, we will present the design methodology for the nested bus-splitting 1-2-3 DDSM3 in detail and simply provide design equations for the bus-splitting 1-3 DDSM3. Note that, in the case of the bus-splitting 1-3 DDSM3, the design equations can be derived from first principles in a similar fashion to the nested bus-splitting 1-2-3 DDSM3.

B. Quantization Noise Contributions of the Nested DDSMs

The output of the nested bus-splitting 1-2-3 DDSM3 can be written as

\[
Y_{123}(z) = \frac{X(z)}{2^{N_1}} + N_1(z) + N_2(z) + N_3(z),
\]

where \( N_1(z) = (1 - z^{-1})^2 \epsilon_Q(z)/(2^{N_{MSB}} + 2^{N_{LSB}+N_{MSB}}) \) is the shaped contribution of the quantizer in the first-order DDSM, \( N_2(z) = (1 - z^{-1})^2 \epsilon_Q(z)/(2^{N_{MSB}} + 2^{N_{LSB}}) \) is the shaped contribution of the quantizer in the second-order DDSM and \( N_3(z) = (1 - z^{-1})^3 \epsilon_Q(z)/(2^{N_{LSB}} + 2^{N_{MSB}}) \) is the shaped contribution from the quantizer in the third order DDSM. Assuming that all quantization noise terms can be modeled as independent additive white sources, we estimate the power spectra of \( N_1(z), N_2(z), \) and \( N_3(z) \) as

\[
S_1(f[k]) = \frac{1}{12L_{\alpha_1}} \left( \frac{1}{2^{N_{MSB}+N_{LSB}}} \right)^2 \\
\times \left[ (1 - z^{-1})^2 e^{-2\pi k/\nu_{\alpha_1}} \right],
\]

\[
S_2(f[k]) = \frac{1}{12L_{\alpha_2}} \left( \frac{1}{2^{N_{LSB}}} \right)^2 \\
\times \left[ (1 - z^{-1})^2 e^{-2\pi k/\nu_{\alpha_2}} \right],
\]

\[
S_3(f[k]) = \frac{1}{12L_{\alpha_3}} \left[ (1 - z^{-1})^3 e^{-2\pi k/\nu_{\alpha_3}} \right].
\]

where \( L_{\alpha_1}, L_{\alpha_2}, \) and \( L_{\alpha_3} \) are the cycle lengths of the quantization error signals from DDSM1, DDSM2, and DDSM3, which are \( 2^{N_{LSB}}, 2^{N_{LSB}+N_{MSB}}, \) and \( 2^{N_{MSB}+N_{LSB}+N_{MSB}} \), respectively (see Appendix B).

C. Error Masking Strategy

The idea of the error masking strategy is to minimize the quantization noise contributions of the bus-splitting DDSM(s) by hiding the noise components \( N_1(z) \) and \( N_2(z) \) below the \( N_3(z) \) component. This idea is illustrated graphically in Fig. 7. The spectral envelopes \( S_1 \) and \( S_2 \) obtained by assuming white quantization noise contributions from the first- and second-order DDSMs should lie below the \( S_3 \) envelope. Since all are discrete spectra, the constraints apply at a finite number of points. In particular, we require that

\[
S_1 < S_3@f = f_s \cdot k/L_{\alpha_1}, \quad k = 1, 2, \ldots, \frac{L_{\alpha_1}}{2},
\]

and

\[
S_2 < S_3@f = f_s \cdot k/L_{\alpha_2}, \quad k = 1, 2, \ldots, \frac{L_{\alpha_2}}{2}.
\]

Recall that, for a DDSM with an output cycle length of \( L_\alpha \), the lowest frequency tone is at \( f_s/L_\alpha \). Therefore, since the cycle lengths for \( N_1 \) and \( N_2 \) are \( 2^{N_{LSB}} \) and \( 2^{N_{LSB}+N_{MSB}} \), the lowest frequency tones in the power spectra of \( N_1 \) and \( N_2 \) are at \( f_s/2^{N_{LSB}} \) and \( f_s/2^{N_{LSB}+N_{MSB}} \), respectively.

Additionally, at the output of the nested 1-2-3 DDSM, since \( S_1 \) and \( S_2 \) are first- and second-order shaped, respectively, while \( S_3 \) is third-order shaped, if the levels of the lowest frequency tones in \( N_1 \) and \( N_2 \) are below that of \( N_3 \), all the tones of \( N_1 \)
and \( N_2 \) should be below the \( S_3 \) envelope. Based on this idea, the constraints can be rewritten as
\[
S_1 < S_0 @ f = f_s / 2^{N_{\text{LSB}}}, \\
S_2 < S_0 @ f = f_s / 2^{N_{\text{MSB}} + N_{\text{LSB}}},
\]
(20)
\( (21) \)

Since
\[
|1 - z^{-1}|^2 = 1 - 2j \sin(\pi f / f_s)^2
\]
(22)
and
\[
\sin(\pi f / f_s) \approx \pi f / f_s \quad \text{for} \quad f \ll f_s,
\]
(23)
we can approximate \( S_1, S_2 \) and \( S_3 \) at low frequencies by
\[
S_1 \approx \frac{1}{12L_{s1}} \cdot \left( \frac{1}{2^{N_{\text{MSB}} + N_{\text{LSB}}}} \right)^2 \cdot 2^2 \left( \frac{\pi f}{f_s} \right)^2,
\]
(24)
\[
S_2 \approx \frac{1}{12L_{s2}} \cdot \left( \frac{1}{2^{N_{\text{MSB}}}} \right)^2 \cdot 2^4 \left( \frac{\pi f}{f_s} \right)^4,
\]
(25)
\[
S_3 \approx \frac{1}{12L_{s3}} \cdot 2^6 (\pi f / f_s)^6.
\]
(26)

Substituting (24)–(26) into the constraints (20) and (21), we obtain
\[
\frac{1}{2^{2N_{\text{MSB}} + 2N_{\text{LSB}}} \cdot 12 \cdot 2^{N_{\text{LSB}}} \cdot \pi^2 \left( 2^{N_{\text{LSB}}} \right)^2} < \frac{1}{12 \cdot 2^{N_{\text{MSB}} + N_{\text{LSB}} + N_{\text{MSB}}} \left( 2^{N_{\text{LSB}}} \right)^6} \quad \text{and}
\]
\[
\frac{1}{2^{2N_{\text{MSB}}} \cdot 12 \cdot 2^{N_{\text{LSB}}} \cdot N_{\text{LSB}} \cdot \pi^2 \left( 2^{N_{\text{LSB}} + N_{\text{LSB}}} \right)^2} < \frac{1}{12 \cdot 2^{N_{\text{MSB}} + N_{\text{LSB}} + N_{\text{MSB}}} \left( 2^{N_{\text{LSB}} + N_{\text{MSB}}} \right)^6},
\]
(27)
(28)

which reduce to
\[
4N_{\text{LSB}} - N_{\text{MSB}} - N_{\text{MSB}} - 4 < 6.6, \\
2N_{\text{LSB}} + 2N_{\text{LSB}} + N_{\text{MSB}} - 2 < 3.3.
\]
(29)
(30)

If we define \( N = N_{\text{MSB}} + N_{\text{LSB}} + N_{\text{LSB}}, M = N_{\text{MSB}} + N_{\text{LSB}} \) and \( L = N_{\text{MSB}}, \) (29) and (30) can be converted to
\[
4N - 5M - 4 < 6.6, \\
2N - 3L - 2 < 3.3.
\]
(31)
(32)

If the wordlength \( N \) of the input is given, \( M \) and \( L \) can be calculated from (31) and (32), respectively. Therefore, the optimized values of \( N_{\text{MSB}}, N_{\text{LSB}} \) and \( N_{\text{LSB}} \) can be calculated using
\[
N_{\text{MSB}} = L, \\
N_{\text{LSB}} = M - L, \\
N_{\text{LSB}} = N - M.
\]
(33)
(34)
(35)

Similar calculations can be performed to determine the optimum wordlengths for the bus-splitting 1–3 DDSM3 and are summarized in Table I.

In order to design a bus-splitting MASH DDSM3 with the same cycle length and similar power spectrum as a conventional \( N_0 \)-bit MASH DDSM3, the procedure is as follows.

- Choose \( N = N_0 + 1 \) to ensure that the output cycle length of the bus-splitting DDSM is the same as that of the conventional \( N_0 \)-bit MASH DDSM [23].

- Choose the desired architecture and determine the optimized wordlengths from Table I using \( M = \left[ (4N - 10.6) / 5 \right] \) and \( L = \left[ (2N - 5.3) / 3 \right] \) where appropriate. Note that \( \lceil x \rceil \) denotes the smallest integer greater than \( x \).

### D. Hardware Requirements

In order to estimate the relative hardware consumption (RHC) of the bus-splitting DDSMs compared to the conventional MASH DDSM3, we adopt the methodology proposed in [14], where the hardware cost of a logic gate is evaluated as half the number of transistors in a conventional CMOS topology, i.e., an inverter costs 1 unit and a NOR gate costs 2 units. In this scheme, a D flip-flop and full adder consume 4 and 14 hardware units, respectively. Furthermore, the hardware cost of the noise cancellation networks in a MASH DDSM2 and a MASH DDSM3 are 18 and 55 units, respectively [14].

In this section, we show in detail how to estimate the RHC of the nested bus-splitting 1–2–3 DDSM3. We also provide a design equation for estimating the RHC of the bus-splitting 1–3 DDSM3. Referring to Fig. 6, the numbers of full adders (\( n_{\text{FA}} \)) and D flip-flops (\( n_{\text{FF}} \)) required to implement the nested bus-splitting 1-2-3 DDSM3 (excluding the noise cancellation networks) are given by
\[
n_{\text{FA}}-123 = N_{\text{LSB}} + 2N_{\text{MSB}} + 4N_{\text{MSB}},
\]
(36)
\[
n_{\text{FF}}-123 = N_{\text{LSB}} + 2N_{\text{MSB}} + 3N_{\text{MSB}}.
\]
(37)

Note that the output of the DDSM1 is a single bit (i.e., 0 or 1). Consequently, when implementing the nested bus-splitting 1-2-3 DDSM3, it is not necessary to instantiate an \( N_{\text{LSB}} \)-bit adder explicitly to combine the output of the DDSM1 with \( X_{\text{LSB}} \). Rather, the addition can be implemented by applying the output of DDSM1 to the carry input of the first accumulator of DDSM2, thus saving hardware.

The total hardware consumption of the nested bus-splitting 1-2-3 DDSM3 (\( \text{HIW}_{123} \)) is given by
\[
\text{HIW}_{123} = 4n_{\text{FA}}-123 + 4n_{\text{FF}}-123 + 73
\]
\[
= 18N_{\text{LSB}} + 36N_{\text{MSB}} + 68N_{\text{MSB}} + 73,
\]
(38)
flip-flops required to implement a conventional $N_0$-bit MASH DDSM3 are given by

$$n_{\text{FF-conv}} = 3N_0$$  \hspace{1cm} (39)

$$n_{\text{FA-conv}} = 3N_0,$$  \hspace{1cm} (40)

respectively. Consequently, the total hardware consumption of the conventional $N_0$-bit MASH DDSM3 is given by

$$\text{HW}_{\text{conv}} = 54N_0 + 55.$$  \hspace{1cm} (41)

Using (31)–(35) and noting that $N = N_0 + 1$, we can estimate the relative hardware consumption of the nested bus-splitting 1-2-3 DDSM3 compared to a conventional structure as

$$\text{RHC}_{123} = \frac{\text{HW}_{123}}{\text{HW}_{\text{conv}}} = \frac{18N_{\text{LSB}} + 36N_{\text{EB}} + 68N_{\text{MSB}} + 73}{54N_0 + 55} \approx \frac{53.7N_0 + 32}{54N_0 + 55} \times 100\%.$$  \hspace{1cm} (42)

Asymptotically, $\text{RHC}_{123}$ approaches 99% from below for large $N_0$ so the 1-2-3 structure provides minimal hardware savings when $N_0$ is large.

In a similar fashion, we can estimate the relative hardware consumption of the bus-splitting 1-3 DDSM3 as

$$\text{RHC}_{13} \approx \frac{46.8N_0 + 25.5}{54N_0 + 55} \times 100\%.$$  \hspace{1cm} (43)

Asymptotically, $\text{RHC}_{13}$ approaches 87% from below for large $N_0$, suggesting that a hardware saving of at least 13% can be expected for typical values of $N_0$.

V. DESIGN EXAMPLES

A. Simulation Results

In order to verify the design methodology described in Section IV, we present a design example for a 19-bit MASH DDSM3. The optimized wordlengths for a bus-splitting 1-3 DDSM3 in this case are $N_{\text{LSB}} = 6$ and $N_{\text{MSB}} = 14$. The optimized wordlengths for a nested bus-splitting 1-2-3 DDSM3 are $N_{\text{LSB}} = 6$, $N_{\text{EB}} = 2$, and $N_{\text{MSB}} = 12$. To compare the conventional and bus-splitting DDSMs, we present simulation results. The inputs of the DDSM are selected as the odd numbers that set the normalized input as close as possible to the value 0.1, i.e., $X = 104857$ in the case of the 14-6-bit bus-splitting 1-3 DDSM3 and 12-2-bit nested bus-splitting 1-2-3 DDSM3 and $X = 52429$ in the case of the 19-bit MASH DDSM3.

First, we simulate the 12-2-6-bit nested bus-splitting 1-2-3 MASH DDSM3 with a constant input to show typical contributions $N_1$, $N_2$, and $N_3$. In Fig. 8, the autocorrelation result confirms that the cycle length of $N_1$ is $2^{19}$ (64). Details of the autocorrelation calculation can be found in Appendix C.

Fig. 9 shows the power spectrum of $N_1$. The power spectra $S_1$ and $S_3$ based on the white noise approximations (16) and (17) are overlaid as well. As expected, the quantization powers are spread over $2^6$ discrete tones, while the location and power of the lowest frequency tone are $f_s/2^6$ and approximately $-146$ dB, respectively. In addition, $N_1$ is shaped by 20 dB/dec, which is the result of the first-order DDSM. Details of the power spectrum calculation can be found in Appendix D.

In Fig. 10, the autocorrelation result confirms that the cycle length of $N_2$ is $2^8$ (256). Fig. 11 shows the power spectrum of $N_2$. The power spectra $S_2$ and $S_3$ based on the white noise approximations (16) and (17) are overlaid as well. As expected, the quantization powers are spread over $2^8$ discrete tones, while the location and power of the lowest frequency tone are $f_s/2^8$ and approximately $-184$ dB, respectively. In addition, $N_2$ is shaped by 40 dB/dec, as expected, for the second-order DDSM.

In Fig. 12, the autocorrelation result confirms that the cycle length of $N_3$ is $2^{20}$. Fig. 13 shows the power spectrum of $N_3$. The power spectrum $S_3$ based on the white noise approximation
Fig. 10. Autocorrelation result for \( N_2 \) when \( N_{1SH} = 6, N_{1MB} = 2, \) and \( N_{MBSH} = 12; \) the input is 104857. The cycle length is \( 2^8 \) (256).

Fig. 12. Autocorrelation result for \( N_3 \) when \( N_{1SH} = 6, N_{1MB} = 2, \) and \( N_{MBSH} = 12; \) the input is 104857. The cycle length is \( 2^9 \).

Fig. 11. Simulated power spectrum for \( N_2 \) when \( N_{1SH} = 6, N_{1MB} = 2, \) and \( N_{MBSH} = 12; \) the input is 104857. The first spur is at \( f_s/2^9 \). The smooth curves are \( S_3(16) \) and \( S_3(17) \).

Fig. 13. Simulated power spectrum for \( N_3 \) when \( N_{1SH} = 6, N_{1MB} = 2, \) and \( N_{MBSH} = 12; \) the input is 104857. The first spur is at \( f_s/2^{10} \). The smooth curve is \( S_3(17) \).

The simulated output power spectrum of the conventional 19-bit MASH DDSM3 is shown in Fig. 14. Its cycle length of \( 2^{20} \) is confirmed by Fig. 15.

The output power spectrum for the 14-6-bit bus-splitting 1–3 DDSM3 is shown in Fig. 16. Note that the \( N_1 \) component lies below the spectral envelope of \( N_3 \) and is therefore masked by it, as expected. Consequently, \( N_1 \) does not adversely affect the overall performance of the DDSM. The cycle length of \( 2^{20} \) is confirmed by Fig. 17. Note that the autocorrelation result for the 14-6-bit bus-splitting 1–3 DDSM3 shown in Fig. 17 displays better randomization of the quantization noise in comparison with the autocorrelation result for the conventional 19-bit MASH DDSM3 shown in Fig. 15.

The output power spectrum for the 12-2-6-bit nested bus-splitting 1-2-3 DDSM3 is shown in Fig. 18. Note that the \( N_1 \) and \( N_2 \) components lie below the spectral envelope of \( N_3 \) and are therefore masked by it, as expected. Consequently, \( N_1 \) and \( N_2 \) do not adversely affect the overall performance of the DDSM. The cycle length of \( 2^{20} \) is confirmed by Fig. 19. Note that the autocorrelation result for the 12-2-6-bit nested bus-splitting 1-2-3 DDSM3 shown in Fig. 19 displays better randomization of the quantization noise in comparison with the autocorrelation result for the conventional 19-bit MASH DDSM3 shown in Fig. 15.

B. Experimental Results

The hardware consumption (HC) for a conventional 19-bit MASH DDSM3 (a) and the bus-splitting DDSM architectures (b) and (c) are summarized in Table II. The HC is reported as the number of flip-flops and the number of four-input lookup tables which represent the synchronous and asynchronous logic, respectively. The total-equivalent-gate (TEG) count for the design is given as well. These results are based on the map report from the Xilinx ISE program [24]. The predicted values for the relative hardware consumption of the bus-splitting architectures given by (42) and (43) are \( RHC_{122} = 97\% \) and \( RHC_{13} = 85\% \). The synthesis results in Table II are consistent with these predictions.
Fig. 14. Simulated power spectrum for a conventional 19-bit MASH DDSM3; the input is 52429. The smooth curve is $S_3(17)$.

Fig. 15. Autocorrelation result for a conventional 19-bit MASH DDSM3; the input is 52429. The cycle length is $2^{20}$.

A logical synthesis flow was constructed with the Synopsys Design Compiler using TSMC 65 nm GP CMOS standard cells. Static timing analysis was performed in PrimeTime. VCD switching activity from a delay-annotated gate-level simulation was annotated onto the netlist in PrimeTime PX, generating peak power waveforms and average power results. The design was constrained so as to minimise power consumption during the synthesis process. Table III shows the area, power, and slack estimates at a clock frequency of 100 MHz. The area synthesis results in Table III are consistent with the theoretical predictions given by (42) and (43).

The 12-2-6-bit nested bus-splitting 1-2-3 DDSM3 consumes more power than the conventional 19-bit MASH DDSM3 although it occupies less digital area. This increase in power consumption is probably caused by the longer critical path of the modulator (the slack is 5.28 ns, as opposed to 6.52 ns in the conventional case) due to the increased amount of combinational logic as shown in Table II. The 14-6-bit 1–3 DDSM3 occupies less digital area and consumes less power than the conventional 19-bit MASH DDSM3, indicating that it is the better option for implementing hardware reduction using the bus-splitting technique.

In order to verify the theoretical and simulated results, we implemented the conventional and bus-splitting MASH DDSMs on a Xilinx Virtex-5 field-programmable-gate-array (FPGA) prototype board clocked at $f_s = 20$ MHz. The modulator outputs were obtained using the Chipscope Pro suite of tools [25], which allow the integration of a logic analyzer within the FPGA. The captured data was subsequently exported to MATLAB for postprocessing. The experimental power spectra of the conventional 19-bit MASH DDSM3, 14-6-bit bus-splitting 1–3 DDSM3, and 12-2-6-bit nested bus-splitting 1-2-3 DDSM3 were obtained and, as expected from the digital nature of the modulators, the experimental results match the simulated results presented in Figs. 14, 16, and 18 exactly.

VI. CONCLUSION

In this paper, we have considered a DDSM with a constant input. Such systems have applications in fractional-N...
frequency synthesizers for generating fixed frequencies. We have presented a design methodology for bus-splitting MASH DDSMs based on error masking which exploits knowledge of the positions of the tones when the input is constant. We have performed a rigorous analysis of the minimal multibit noise shaping concept conceived by Norsworthy et al. [17] and we have extended it to the nested bus-splitting architecture.

Using the bus-splitting technique, hardware savings of at least 13% can be achieved in the undithered case with constant input compared to a standard DDSM3 architecture. This hardware reduction can be achieved without sacrificing the spectral performance of the modulator. In Part II, we will address by simulation the performance of bus-splitting DDSMs with nonconstant inputs.

APPENDIX A

Consider the bus-splitting 1–3 DDSM3 shown in Fig. 4 with a constant input. The cycle length of the quantization error of DDSM1 is given by [27]

\[ L_{a1} = \frac{M_1}{\gcd(M_1, X_{\text{LSB}})}, \]  

where \( M_1 = 2^{N_{\text{LSB}}} \) and \( \gcd(x, y) \) denotes the greatest common divisor of \( x \) and \( y \). Consequently, when the LSB of the input is set to 1, the cycle length of the first stage is given by \( L_{a1} = 2^{N_{\text{LSB}}} \) and the first tone occurs at a frequency \( f_1 = f_s/2^{N_{\text{LSB}}} \). The negative of the quantization error of the first stage of DDSM3 can be written as

\[
-\varepsilon_{31}[n] = (y_1[n] + X_{\text{MSB}} - \varepsilon_{31}[n - 1]) \mod M_2 \]
\[
= \left( -\varepsilon_{31}[0] + \sum_{k=1}^{n} (y_1[k] + X_{\text{MSB}}) \right) \mod M_2, \tag{45}
\]

where \( y_1[n] \) is the output from DDSM1 and \( M_2 = 2^{N_{\text{MSB}}} \). As \( -\varepsilon_{31}[n] \) is periodic, \( -\varepsilon_{31}[0] = -\varepsilon_{31}[L_{a31}] \), where \( L_{a31} \) is the cycle length of the first stage of DDSM3. We can rewrite (45) as

\[
\left( \sum_{n=1}^{L_{a31}} y_1[n] + X_{\text{MSB}} \right) \mod M_2 = 0. \tag{46}
\]

Imposing the condition that \( L_{a31} = b \cdot L_{a1} \), where \( b \) is an integer, we obtain

\[
b \cdot \left( \sum_{n=1}^{L_{a1}} y_1[n] + X_{\text{MSB}} \right) \mod M_2 = 0, \tag{47}
\]

Using the fact that

\[
\frac{1}{L_{a1}} \sum_{n=1}^{L_{a1}} y_1[n] = \frac{X_{\text{LSB}}}{M_1}, \tag{48}
\]

we obtain

\[
b \cdot \left( L_{a1} \frac{X_{\text{LSB}}}{M_1} + L_{a1} \cdot X_{\text{MSB}} \right) \mod M_2 = 0. \tag{49}
\]
Using (44), we note that the first term of (49) is odd. Consequently, \( b \) should be equal to \( M_2 \) to satisfy (49) and the cycle length of the first stage in the DDSM3 is \( L_{s31} \cdot M_2 \).

As the quantization error \( e_{22}[n] \) of the second stage of the DDSM3 is also periodic, the relation

\[
\left( \sum_{n=1}^{L_{s2}} -e_{31}[n] \right) \mod M_2 = 0,
\]

should be satisfied, where \( L_{s32} \) is the cycle length of the second stage of the DDSM3. Imposing the constraint that \( L_{s32} = c \cdot L_{s31} \), where \( c \) is an integer, we obtain

\[
c \cdot \left( \sum_{n=1}^{L_{s1}} -e_{31}[n] \right) \mod M_2 = 0.
\]

Substituting \(-e_{31}[n]\) from (45) yields

\[
c \cdot \left( \sum_{n=1}^{M_2 L_{s1}} \left( \sum_{k=1}^{n} (y_1[k] + X_{\text{MSB}}) - e_{31}[0] \right) \right) \mod M_2 = 0.
\]

Since \((y_1[k] + X_{\text{MSB}})\) is periodic, we have the following according to Lemma 2 in [10]:

\[
\left( \sum_{n=1}^{M_2 L_{s1}} \left( \sum_{k=1}^{n} y_1[k] + X_{\text{MSB}} \right) \right) \mod M_2 = 0.
\]

Moreover, the modulo operation of \(-M_2 L_{s1} e_{31}[0]\) is zero. Consequently, \( c \) should be equal to 1 to satisfy (52) and the cycle length of the second stage of DDSM3 is equal to the cycle length of the first stage and is given by \( L_{s1} \cdot M_2 \).

We can generalize this result to prove that the cycle length at the output of a bus-splitting 1-D DDSM1 is equal to \( L_{s1} \cdot M_2 \) i.e., increasing the order of the DDSM1 by cascading additional first-order stages does not increase the cycle length. Since the quantization error of the \( l \)th stage is periodic, we obtain the relation

\[
\left( \sum_{n=1}^{L_{s1}} -e_{l-1}[n] \right) \mod M_2 = 0.
\]

The quantization error of the \((l-1)\)th stage is also periodic and we can rewrite (54) as

\[
d \cdot \left( \sum_{n=1}^{L_{s1}} -e_{l-1}[n] \right) \mod M_2 = 0,
\]

where \( d \) is an integer. The quantization error of the \((l-1)\)th stage is replaced with the summation of the input of the \((l-1)\)th stage, yielding

\[
d \cdot \left( \sum_{n=1}^{M_2 L_{s1} - 2} \left( \sum_{k=1}^{n} e_{l-2}[k] - e_{l-1}[0] \right) \right) \mod M_2 = 0.
\]

Since \( e_{l-2}[k] \) is periodic, we have the following according to Lemma 2 in [10]:

\[
\left( \sum_{n=1}^{M_2 L_{s1} - 2} \left( \sum_{k=1}^{n} e_{l-2}[k] \right) \right) \mod M_2 = 0.
\]

Moreover, the modulo operation of \(-M_2 L_{s1} e_{l-1}[0]\) is zero. Consequently, \( d \) should be equal to 1 to satisfy (56) and the cycle length is equal to \( L_{s1} \cdot M_2 \). Note that, when the input is odd, the cycle length of the quantization noise at the outputs of DDSM1 and DDSM3 in the bus-splitting 1–3 DDSM3 are given by \( 2(N_{\text{LSB}} + N_{\text{MSB}}) \) and \( 2(N_{\text{LSB}} + N_{\text{MSB}}) \), respectively.

**APPENDIX B**

Consider the nested bus-splitting 1-2-3 DDSM3 shown in Fig. 6 with a constant input. When the LSB of the input is set to 1, the cycle lengths of the quantization errors from DDSM1 and DDSM2 using (44) and (57) are given by \( L_{s1} = 2^{N_{\text{LSB}}} \) and \( L_{s2} = 2^{N_{\text{LSB}}} + 2^{N_{\text{MSB}}} \), respectively. The negative of the quantization error of the first stage of DDSM3 can be written as

\[
-e_{31}[n] = (y_2[n] + X_{\text{MSB}} - e_{31}[n-1]) \mod M_3
\]

\[
= (-e_{31}[0] + \sum_{k=1}^{n} y_2[k] + X_{\text{MSB}}) \mod M_3,
\]

where \( y_2[n] \) is the output from DDSM2 and \( M_3 = 2^{N_{\text{MSB}}} \). As \( -e_{31}[n] \) is periodic, \( -e_{31}[0] = -e_{31}[L_{s31}] \), where \( L_{s31} \) is the cycle length of the first stage of DDSM3. We can rewrite (58) as

\[
\left( \sum_{n=1}^{L_{s31}} y_2[n] + X_{\text{MSB}} \right) \mod M_3 = 0.
\]

Imposing the condition that \( L_{s31} = b \cdot L_{s2} \), where \( b \) is an integer and \( L_{s2} \) is the cycle length of the quantization error of DDSM2, we obtain

\[
b \cdot \left( \sum_{n=1}^{L_{s2}} y_2[n] + X_{\text{MSB}} \right) \mod M_3 = 0.
\]

Using the fact that

\[
\frac{1}{L_{s2}} \sum_{n=1}^{L_{s2}} y_2[n] = X_{\text{MSB}} + \frac{X_{\text{LSB}}}{M_1} + N_2 \cdot X_{\text{MSB}}
\]

we obtain

\[
b \cdot \left( \frac{X_{\text{MSB}} + \frac{X_{\text{LSB}}}{M_1} + N_2 \cdot X_{\text{MSB}}}{M_2} \right) \mod M_3 = 0.
\]

Simplifying (62) yields

\[
b \cdot \left( \frac{L_{s1} X_{\text{MSB}}}{M_1} + L_{s1} \cdot X_{\text{LSB}} + L_{s2} \cdot X_{\text{MSB}} \right) \mod M_3 = 0.
\]

(63)
Using (44), we note that the first term of (63) is odd. Consequently, \( b \) should be equal to \( M_3 \) to satisfy (63) and the cycle length of its first stage in the DDSM3 is \( L_{S2} \cdot M_3 \). Thus \( L_{S2} = 2^{N_{EB}} + 2^{N_{MB}} + 2^{N_{MB}} \).

As the quantization error \( e_{31}[n] \) of the second stage of the DDSM3 is also periodic, the relations (50) and (51) also hold for the case of the nested bus-splitting 1-2-3 DDSM3. Substituting \( -e_{31}[n] \) from (58) into (51) yields
\[
c \cdot \left( \sum_{n=1}^{M_3 \cdot L_{S2}} \left( \sum_{k=1}^{n} (y_p[k] + X_{MSB}) - e_{31}[0] \right) \right) \mod M_3 = 0,
\]
where \( c \) is an integer. Since \((y_p[k] + X_{MSB})\) is periodic, we have the following zero according to Lemma 2 in [10]
\[
\left( \sum_{n=1}^{M_3 \cdot L_{S2}} \left( \sum_{k=1}^{n} (y_p[k] + X_{MSB}) \right) \right) \mod M_3 = 0.
\]
Moreover, the modulo operation of \(-M_3 L_{S2} e_{31}[0]\) is zero. Consequently, \( c \) should be equal to 1 to satisfy (64) and the cycle length of the second stage of DDSM3 is equal to the cycle length of the first stage and given by \( L_{S2} \cdot M_3 \).

This result can be generalized in a similar manner to the bus-splitting 1–3 DDSM3 case to prove that, when the input is constant, the cycle length at the output of a nested-bus-splitting 1-2-1 DDSM is equal to \( L_{S2} \cdot M_3 \). Thus, increasing the order of DDSM by cascading additional first-order stages does not increase the cycle length.

**APPENDIX C**

The DDSM is a deterministic finite-state machine (FSM). It always produces a periodic output sequence (cycle) when the input is a constant. In order to evaluate the cycle length, we obtain an unbiased estimate of the autocorrelation sequence of the quantizer error from a time-domain simulation of the DDSM with \( 2^Q \) output samples. An unbiased estimate of a finite record of length \( Q \) of a random signal \( x[n] \) is given by [26]
\[
\hat{\phi}_{xx}[m] = \left( \frac{1}{Q - |m|} \right) \sum_{n=|m|}^{Q-1} x[n] x[n + |m|].
\]
This has been implemented in MATLAB using the \textit{xcorr} function with the \textit{unbiased} option. The dc component of the data to be analyzed is removed prior to the application of the \textit{xcorr} function and the results are normalized such that the autocorrelation at zero lag is 1.

**APPENDIX D**

The simulation results in Section V show the discrete power spectrum \( P[k] \) of the output \( y \) of the DDSM defined by
\[
P[k] = |Y[k]|^2,
\]
where \( Y[k] \) is the discrete-time Fourier series of the output of the DDSM with its dc term removed given by
\[
Y[k] = \frac{1}{L_S} \sum_{k=0}^{L_S-1} y[n] e^{-j2\pi kn/L_S},
\]
Note that the discrete power spectrum of a sequence with period \( L_S \) consists of \( L_S \) discrete tones.

**REFERENCES**

Brian Fitzgibbon (S’06) received the B.E. degree in electrical and electronic engineering from the University College Cork, Ireland, in 2009. He is currently working toward the Ph.D. degree in the Department of Electrical and Electronic Engineering and Tyndall National Institute, University College Cork.

Michael Peter Kennedy (S’84–M’91–SM’95–F’98) received the B.E. degree in electronics from the National University of Ireland, Dublin, in 1984, the M.S. and Ph.D. degrees from the University of California (UC Berkeley), Berkeley, in 1987 and 1991, respectively, and the D.Eng. degree from the National University of Ireland in 2010.

He worked as a Design Engineer with Philips Electronics, a Postdoctoral Research Engineer at the Electronics Research Laboratory, UC Berkeley, and as a Professeur Invité at the Federal Institute of Technology Lausanne (EPFL), Switzerland. From 1992 to 2000, he was on the faculty of the Department of Electronic and Electrical Engineering at University College Dublin (UCD), Dublin, Ireland, where he taught electronic circuits and computer-aided circuit analysis and directed the undergraduate Electronics Laboratory. In 2000, he joined University College Cork (UCC), Cork, Ireland, as Professor and Head of the Department of Microelectronic Engineering. He was Dean of the Faculty of Engineering at UCC from 2003 to 2005 and was Vice-President for Research from 2005 through 2010. He has published over 300 papers in the area of nonlinear circuits, holds six patents, and has taught courses on nonlinear dynamics and chaos in England, Switzerland, Italy, and Hungary. His research interests are in the simulation, analysis, and design of nonlinear dynamical systems for applications in communications and signal processing.

Dr. Kennedy was the recipient of the 1991 Best Paper Award from the International Journal of Circuit Theory and Applications and the Best Paper Award at the European Conference on Circuit Theory and Design 1999. He served as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS from 1993 to 1995 and from 1999 to 2004. He was awarded the IEEE Third Millennium Medal, the IEEE Circuits and Systems Society Golden Jubilee Medal in 2000, and the inaugural Parsons Medal for Engineering Sciences by the Royal Irish Academy in 2001. He was elected to membership of the Royal Irish Academy in 2004. He was Vice-President for Region 8 of the IEEE Circuits and Systems Society from 2005 to 2007. He was made an IEEE Fellow in 1998 for his contributions to the study of neural networks and nonlinear dynamics.

Franco Maloberti (SM‘87–F’96) received the Laurea degree in physics (summa cum laude) from the University of Parma, Parma, Italy, in 1968, and the Doctorate Honoris Causa in electronics from the Instituto Nacional de Astrofisica, Optica y Electronica (Inaoe), Puebla, Mexico, in 1996.

He was the TI/J.Kilby Chair Professor at Texas A&M University and the Distinguished Microelectronic Chair Professor at the University of Texas at Dallas. He was a Visiting Professor at The Swiss Federal Institute of Technology (ETH-PEL), Zurich, Switzerland and at the EPFL, Lausanne, Switzerland. Currently he is Microelectronics Professor, Head of the Micro Integrated Systems Group, University of Pavia, Italy, and Honorary Professor, University of Macau, China. His professional expertise is in the design, analysis, and characterization of integrated circuits and analog digital applications, mainly in the areas of switched-capacitor circuits, data converters, interfaces for telecommunication and sensor systems, and CAD for analog and mixed A/D design. He has written more than 400 published papers on journals or conference proceedings and four books, and holds 30 patents.