SWITCHED-CAPACITOR CIRCUITS WITH LOW OP-AMP GAIN SENSITIVITY

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ABSTRACT

Switched capacitor integrator and amplifier stages are discussed which are compensated for both dc offset and finite op-amp gain effects. This makes the use of simple single-stage amplifiers possible even in high-selectivity and/or high-accuracy circuits, and hence may allow the extension of the frequency range of switched-capacitor filters, amplifiers and data converters beyond its current limits.

INTRODUCTION

An important limitation on the extension of the operation of switched-capacitor (SC) filters to higher frequencies is due to the reduced dc gain $A$ of the op-amps which can provide wider band-widths. This reduction results in op-amp input voltages $V_i = -V_{out}/A$ which are no longer negligible, and hence the response of stages whose operation depends critically on the presence of a virtual ground at the op-amp inputs is seriously distorted. If the clock frequency is much higher than the signal frequency, then $V_{out(n)}$ can be regarded as a constant during the clock half-cycles when the output is sampled. If in addition $V_i$ is held at this same value also during the other ("hold") half-cycles, then $V_{out}$ can be regarded as a dc offset voltage, and hence it can be reduced by using available schemes aimed at offset voltage elimination. This perceptive observation was made recently by Nagaraj et al. (1), who also suggested an offset-compensated integrator circuit (Fig. 1) based on the noise-cancelling integrator of Lam and Copeland (2).

The purpose of this paper is to suggest alternative circuits, originally proposed by the authors as offset-cancelled low-slew-rate integrators (3,4), for applications in which low-dc-gain op-amps must be used. The finite-gain operations of these circuits are analyzed from both physical and mathematical viewpoints, and their properties are compared with those of the circuit proposed in Ref. 1.

LOW GAIN-SENSITIVITY INTEGRATORS

Two offset-compensated inverting SC integrators (3,4) are shown in Figs. 2 & 3. Both have the requisite property that $V_{out}$ changes only by a small amount $\Delta V_{out}$ between the "sample" ($\phi_2 = 1$) and the "hold" ($\phi_1 = 1$) periods. A general scheme representing both circuits, as well as that suggested earlier by Gregorian (7), is shown in Fig. 4. In this circuit, $C_1$ & $C_2$ are never disconnected from the input terminal of the op-amp, and hence the charge conservation equation at this terminal gives

$$C_1 [V_{in(n)} - V_{A(n)} + V_{p(n-1/2)]} + C_2 [V_{out(n)} - V_{out(n-1)} + V_{p(n-1/2)]} = 0.$$  

The input-output relation is therefore

$$V_{out(n)} - V_{out(n-1)} = -C_1/C_2 \cdot V_{in(n)} - V_{A(n-1)} + C_1/C_2 \cdot [V_{A(n)} - V_{A(n-1)}],$$

where $z = \exp(j\omega T)$, the first error term is $V_{out}(z) \cdot 1/z$, and the second error term is $-C_1/C_2 \cdot V_{out}(z)/A$, which is very small since $1/A \omega < 1$. The second error term depends on the structure of the SC feedback circuit SCC. For the circuit of Fig. 3, $V_{out(n-1/2)} = V_{A(n-1)}$ and hence the second error term is $-C_1/C_2 \cdot V_{out(n-1/2)}$, which is normally even smaller than the first one since $C_1/C_2$ is usually smaller than 1.

By contrast, for the simpler circuit of ref. 5, $V_{out(n-1/2)} = 0$, and hence the second error term is $-C_1/C_2 \cdot V_{out(n-1)}$, which can be appreciable. This analysis illustrates how the process of keeping $V_{A}$ constant reduces the finite-gain error. Detailed calculations (6) give the results shown in Table 1, where the expressions for the gain error $m(u)$ and phase error $\phi(u)$ are displayed. These errors are defined (5) by the relation $H(u) = H_1(u) + m(u) \cdot \exp[j \cdot \phi(u)]$, where $H_1(u)$ is the ideal (infinite-gain) response and $H(u)$ is the actual (finite-gain) one. The formulas of Table 1 were derived using the assumptions that $u \omega T = 1$ and $u \omega T = 1/A < 1$, and give good accuracy over the broad frequency range $0.05f_0 < f < 3f_0$, where $f_0 = (f_{DC}/2C_2)$ is the unity-gain frequency of the integrator (5).

Fig. 5 illustrates the error responses computed directly from the circuits for $A = 100$, $C_1/C_2 = 0.2$, $f_0 = 1/T = 100$ kHz and hence $f_0 = 4.19$ kHz. They are in good agreement with the values predicted by the formulas of Table 1.

For the offset-compensated noninverting integrator described in ref. 4, the gain error is the same, while the phase error is twice as large, as for the inverting integrator of Fig. 3. An inspection of Table 1 and Fig. 5a shows, the gain error is lowest (<0.02 dB in Fig. 2a) for the integrator of ref. 1. The integrators of refs. 3 & 4 give a larger gain error, 0.1-0.12 dB in Fig. 5a. This is comparable to the gain error of the uncompensated integrator. The situation is

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reversed, however, for the phase error. As both the formulas and curves indicate, the errors of the integrators of Figs. 2 & 3 are very small; for the circuit of Fig. 2 (with \( C_2 = C_3 \)), the error is around 0.03°, while for that of Fig. 3, it is approximately 0.006°. The error of the uncompensated integrator is around 0.6° near \( f_0 \), while that of the circuit of Fig. 1 is close to 0.1°. The gain error of the integrator is equivalent to an element-value variation \( \Delta C \), while the phase error corresponds to a finite-Q effect, for both biquad and ladder SC filter circuits (3). Hence, the finite-gain effect in SC circuits using the integrators of Figs. 2 & 3 is a slight shift in the frequency response. If \( n \) is known, the value of \( C_2 \) can be replaced by \( C_2[1-n] \) in all integrators, thereby essentially eliminating all finite-gain effects. By contrast, the use of the circuit of ref. 1 results in a peaking due to the negative phase error, and hence the negative Q of the integrators.

The above statements are illustrated by the responses of a fifth-order elliptic SC filter, shown in Fig. 6. For a biquad built from offset-compensated integrators, the ideal and finite-gain responses are compared in Fig. 7. Again, the finite-gain effect is essentially a slight shift of the response along the frequency axis, without any noticeable change in the effective pole-Q.

**LOW GAIN-SENSITIVITY AMPLIFIERS AND DATA CONVERTERS**

The application of the compensation principle of Figs. 1-4 to SC amplifiers (4), as used in AGC circuits, voltage amplifiers and data converters, is illustrated in Fig. 8. Assuming that the clock phases shown without parentheses are valid at the input switches, it can readily be shown that the input/output relation is \( V_{\text{out}}(n) = -(C_1/C_2) V_{\text{in}}(n) + (1 + C_1/C_2) V_A(n - 1/2) \). Since \( C_2 \) and \( C_1 = C_4 \) trade places between the "sample" and "hold" periods, it can easily be seen that \( V_{\text{out}} \) changes by \( -V_{\text{in}}/A \) when \( \phi_1 = 0 \), and hence \( V_{\text{out}}(n) = V_A(n - 1/2) \). A similar derivation for the uncompensated amplifier, or for the amplifier using the scheme of ref. 7, reveals that for those circuits the error term is proportional to \( -V_{\text{out}}/A \). Hence, the offset compensation effectively replaces the op-amp gain \( A \) by \( A^2 \). In fact, detailed calculations show that the dc gain of the circuit of Fig. 8 is given by

\[
H(z) \bigg|_{z=1} = \frac{-C_1/C_2}{1 + (1 + C_1/C_2) v^2}
\]

while that of an uncompensated amplifier (or one using the scheme of ref. 7) is

\[
H_{uc}(z) \bigg|_{z=1} = \frac{-C_1/C_2}{1 + (1 + C_1/C_2) v^2}
\]

Fig. 9 compares the resulting gain responses of three amplifiers, each with a nominal voltage gain of 2 (i.e., 6.02 dB), and with a clock frequency of 100 kHz. Clearly, for \( A = 100 \), the gain error of the compensated amplifier is less than 0.02 dB, up to about 6 kHz. For the uncompensated circuit, the error is more than 0.2 dB at all frequencies.

**CONCLUSIONS**

On the basis of the results presented, it appears that all three integrators analyzed can reduce the finite-gain sensitivity of SC circuits considerably. There are, however, appreciable differences between them. The circuit of Fig. 2 is the simplest and it can be used either as an inverting or noninverting integrator, by choosing appropriate phasing for the input switches. Its gain and phase errors, for \( C_1 = C_3 \), are small and nearly constant. The circuit of Fig. 3, when used with a single-input inverting integrator, is simple; however, for \( n \) inputs \( C_n \) must be replaced by \( p \) capacitors. Also, for noninverting operation, the circuit must be modified as described in ref. 4. The gain error of the circuit of Fig. 3 is small, and its phase error is essentially zero. The gain error of the noninverting circuit (4) is the same for the inverting integrator; its phase error is twice as large.) Thus, all these circuits can be useful for high-Q filtering applications. The circuit in Fig. 1 is more complicated than those in Figs. 2 & 3, and is not fully insensitive. Also, since both terminals of \( C_4 \) are connected to sensitive high-impedance nodes during the \( \phi_1 = 0 \) interval, this stage is likely to be susceptible to substrate noise coupling via the bottom plate of \( C_3 \). The circuit has essentially no gain error, and an appreciable negative phase shift. Hence, it may be most useful in low-Q applications, and/or when \( f_0/f_c < 0.01 \).

For SC amplifiers, the low-gain-sensitivity property of the compensated circuits remains valid. For these circuits, the low-slew-rate offset compensation effectively squares the op-amp gain, making possible the operation of high-accuracy AGC amplifiers, DACs, etc. with op-amps having dc gains as low as 100. This may enable the designer to use wide-band single-stage op-amps at high clock rates.

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**REFERENCES**


![Fig. 1. The offset- and gain-compensated amplifier of ref. 1](image1)

![Fig. 2. The compensated integrator of ref. 3](image2)

![Fig. 3. The compensated inverting integrator of ref. 4](image3)

![Fig. 4. General scheme of the offset-compensated integrators of refs. 3, 4 & 7](image4)

![Fig. 5a. Error responses of SC integrators: (I) Fig. 1; (II) Fig. 2; (III) Fig. 3; (IV) uncompensated integrator. C1/C2 = 0.3, f2 = 100 kHz](image5a)
Fig. 5. Error responses of SC integrators: (I) Fig. 3; (II) Fig. 2; (III) Fig. 1; (IV) uncompensated integrator. $C_1/C_2 = 0.2$, $f_c = 100$ kHz.

Fig. 6. Ladder filter gain responses:
(1) ideal; (II) $A = 100$, uncompensated; (III) $A = 100$, using for inverting integrators the circuit of Fig. 3 and for non-inverting integrators the circuit of Fig. 2; (IV) $A = 100$, using the circuit of Fig. 1. $f_c = 64$ kHz.

OK for GaAs

CDS without glitching is not possible.

Fig. 7. The loss response of the ladder of Fig. 6 with infinite and finite-gain op-amps.

Fig. 8. Offset- and gain-compensated SC amplifier.

Fig. 9. Gain responses of the SC amplifier: (I) ideal; (II) using the circuit of Fig. 6; (III) uncompensated; $f_c = 100$ kHz, $A = 100$, $C_1 = 2C_2 = 2C_4/3$. 

800