ADC CHARACTERISATION USING THE CODE DENSITY TEST METHOD WITH DETERMINISTIC SAMPLING

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ABSTRACT

This paper describes a novel approach for ADC characterisation that uses the code density test method while overcoming the request of a huge number of samples. Instead of collecting samples with a clock frequency uncorrelated with the input test signal, we propose a deterministic sampling controlled by a PLL locked to the input test signal frequency.

1 INTRODUCTION

As new generations of A/D converters provide increasing speed and resolution, they need new methods for characterisation under operating conditions. The Code Density Test (CDT) method allows a full characterisation of ADCs, but it needs a huge number of samples. Indeed, the CDT method requires: (i) an input waveform with well-known amplitude distribution (usually a full-scale sinusoid with ultra-low distortion) and (ii) a sampling rate uncorrelated with the input signal period. Under these assumptions, the statistical distribution of collected samples corresponds to the real amplitude histogram, and ADC non-idealities are extracted from the deviation of the actual histogram from the ideal one [1].

Since clock and input signal generators are uncorrelated, the histogram of collected samples tends asymptotically to the histogram of the ADC when the number of samples increases, so the accuracy of the method depends on the number of samples acquired. For instance, let us consider an n-bit ADC whose precision is $\beta$ LSB. To estimate the differential non-linearity (DNL) within $(1 - \alpha) 100$% confidence interval, the minimum number of samples is [1]:

$$\mathcal{N}_s = \frac{Z_{\alpha/2}^2 \pi 2^{n-1}}{\beta^2},$$

(1)

where $Z_{\alpha/2}$ is the value of the variable in the standard normal distribution function for which the confidence level is $1 - \alpha$ [2].

To evaluate the DNL with accuracy $\beta = 0.1$ LSB and $\alpha = 0.05$, we need 268,000 samples for an 8-bit converter and 68,500,000 samples for a 16-bit converter. Those figures lead to an impractical

This work has been supported by the European Union under the ESPRIT Basic Research Project 8820 – AMATIST.
amount of data. Therefore this testing method is not suitable for industrial use, especially for high-resolution slow-speed ADCs.

To overcome the problem mentioned above, we propose to use a deterministic sampling controlled by the input signal frequency through a phase-locked loop (PLL). We will see that a suitable choice of the sampling time instants allows us to reduce significantly the number of samples required for the ADC characterisation.

2 CODE DENSITY TEST METHOD WITH DETERMINISTIC SAMPLING

In the CDT method, the knowledge of the input amplitude distribution allows us to estimate the number of digital output samples that will fall into a given bin. Any deviation from the predicted number of samples denotes a DNL error. The set of samples that fits CDT requirements can be collected using two methods. The first one is the conventional stochastic sampling described in the introduction. A second method consists in gathering samples corresponding to sampling times known and uniformly distributed within the period $T$ of the input test signal. The number of samples required to characterise an $n$-bit ADC can be found using the amplitude distribution of the test signal.

For simplicity, let us consider an ADC with a symmetrical input range $[-V_{ref}, +V_{ref}]$, fed with a sine wave $A \sin 2\pi f_s t$. The probability that a sample lies into the $i$-th bin is [1]:

$$P(i, A) = \frac{1}{\pi} \left( \sin^{-1} \left( \frac{2i - 2^n - 1}{2^n} \cdot \frac{V_{ref}}{A} \right) - \sin^{-1} \left( \frac{2i - 2^n - 3}{2^n} \cdot \frac{V_{ref}}{A} \right) \right). \tag{2}$$

The minimum probability corresponds to a zero input or bin $i = 2^{n-1}$:

$$P(2^{n-1}, A) = \frac{2}{\pi} \sin^{-1} \left( \frac{V_{ref}}{2^n A} \right). \tag{3}$$

To ensure the presence of at least $k$ samples in every bin, the minimum number of samples $N_s$ to be collected is:

$$N_s = \frac{k}{P(2^{n-1}, A)} = \frac{\pi k}{2 \sin^{-1} \left( \frac{V_{ref}}{2^n A} \right)}. \tag{4}$$

For a full-scale input signal with amplitude $A = V_{ref}$, eq. (4) becomes:

$$N_s = \frac{\pi k}{2 \sin^{-1} \left( 2^{-n} \right)}. \tag{5}$$

In practical situations, a resolution of 0.1 bit in the DNL measurement can be considered satisfactory. This requires at least 10 samples per bin for an ADC characterisation. However, we must consider that in real systems the sampling time is affected by some jitter. Because of the sampling jitter we can have a moving in (or out) of samples at the periphery of the bin. If we are able to limit this effect to only two moved samples, we achieve a DNL accuracy equal or better than $\pm 0.2$ LSB. Industrial tests normally require a 0.5 LSB resolution; therefore, the above choice seems to be a proper one.

Table I compares the number of samples needed for CDT for random and deterministic sampling methods. For both methods, the accuracy was $\beta = 0.2$ LSB. The confidence level for random
TABLE I. NUMBER OF SAMPLES REQUIRED FOR THE CDT METHOD.

<table>
<thead>
<tr>
<th>$n$</th>
<th>random</th>
<th>deterministic</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>67,000</td>
<td>4,022</td>
</tr>
<tr>
<td>10</td>
<td>267,500</td>
<td>16,085</td>
</tr>
<tr>
<td>12</td>
<td>1,050,000</td>
<td>64,340</td>
</tr>
<tr>
<td>14</td>
<td>4,282,500</td>
<td>257,360</td>
</tr>
<tr>
<td>16</td>
<td>17,125,000</td>
<td>1,029,437</td>
</tr>
</tbody>
</table>

sampling was $1 - \alpha = 0.95$. In the deterministic method, 10 samples per bin were considered. From Table I, we can see that deterministic sampling reduces the number of required samples by a factor 16 with respect to random sampling.

To obtain a deterministic sampling with given timing, the master clock has to be synchronised with the input signal, and its frequency must be $N_s$ times the one of the input signal:

$$f_{ck} = N_s \cdot f_s.$$ \hfill (6)

This requirement can be fulfilled with a digital PLL, which ensures the proper clock operation and, in addition, guarantees the tracking of the input signal $V_{in}$ even in case of drifts due to temperature and long-term variations. A smart sampling block manages the sample collection, which can be spread over a suitable number of periods of the input signal, according to the speed characteristics of the device under test (DUT).

Fig. 1 shows a possible implementation of the characterisation system. It is worth noting that the proposed method allows us to use an ultra-low distortion oscillator without the need of precise frequency tuning, because we track it with the acquisition control section.

![Diagram](attachment:image.png)

Fig. 1. Scheme of the ADC characterisation system.
3 SIMULATION RESULTS

To verify the proposed characterisation method, the test of an ideal 10-bit ADC has been simulated with MATLAB, taking 16,085 samples to have at least 10 samples in every bin. Fig. 2 (a) shows the resulting histogram. The test of an ADC with a DNL equal to 0.5 LSB (affecting a single bin: the bin 511) has been simulated for comparison. The resulting histogram is plotted in Fig. 2 (b).

4 PERFORMANCE REQUIREMENTS

As we have seen above, the proposed method requires an ultra-low distortion oscillator to generate the input test signal with suitable accuracy. This component is a key point of the system, because any non-ideality in the input sine wave results in a measurement error.

A second key block is the sample-and-hold, which must have enough speed and accuracy to not degrade the signal entered into the ADC.

To evaluate the requirements for the clock, let us consider the input signal in time domain, as shown in Fig. 3. The clock jitter may cause the samples at extremes of time interval to be shifted to neighboring bins. The accuracy $\beta$ (in LSB) is related to clock jitter $T_j$ through the following relationship:

$$\beta = \frac{2 \cdot T_j}{k \cdot T_{ck}}$$  \hspace{1cm} (7)

where $T_{ck}$ is the sampling period, i.e. the interval between two consecutive samples. The factor 2 accounts for the possible shift of samples at both ends of the interval.

Since $T_{ck} = \frac{1}{f_{ck}}$ is related to $N_s$ by eq. (6) and then to $k$ by eq. (5), the accuracy $\beta$ results to be insensitive to the number of samples in every bin. Indeed, eq. (7) can be written as:

$$\beta = \frac{T_j}{T} \cdot \frac{\pi}{\sin^{-1}(2^{-n})}$$  \hspace{1cm} (8)
where \( T \) is the input signal period: \( T = \frac{1}{f_s} \).

Eq. (8) can be used to determine the maximum jitter \( T_{j,\text{max}} \) which can be tolerated for a given accuracy:

\[
T_{j,\text{max}} = \beta T \cdot \frac{\sin^{-1}(2^{-n})}{\pi} = \beta T \cdot \frac{2^{-n}}{\pi}.
\] (9)

The approximation \( \sin^{-1}(2^{-n}) = 2^{-n} \) is reasonable for \( n > 1 \). Fig. 4 shows the values of \( T_{j,\text{max}} \) as a function of ADC resolution, for an input signal with period \( T = 1 \text{ ms} \) and for different values of accuracy \( \beta \). We can see that clock jitter requirements are tight only for high-resolution converters.

Finally, to define PLL requirements, let us consider the schematic diagram in Fig. 5 [3]. The VCO conversion gain is:

\[
K_0 = \frac{\Delta f_{\text{ck}}}{\Delta V_c}.
\] (10)

Assuming a linear relationship between the control voltage \( V_c \) and the output frequency \( f_{\text{ck}} \), the VCO gain \( K_0 \) is constant. When the PLL is in the locked state, its accuracy is limited by fluctuations of \( V_c \), which introduce a sampling jitter. The relationship between control voltage fluctuation \( \Delta V_c \) and sampling jitter \( T_j \) is:

\[
\Delta V_c = \frac{T_j}{K_0 T (T + T_j)} = \frac{T_j}{K_0 T^2}.
\] (11)

From eq. (10), we can see that operating frequency range of the VCO is increased by large values of \( K_0 \), while noise insensitivity is improved by lowering \( K_0 \). Therefore a trade-off between frequency range and noise immunity must be pursued.
5 CONCLUSION

We have shown that a deterministic collection (opposed to a stochastic one) greatly reduces the number of samples required for ADC characterisation with the CDT method. This extends the applicability of the CDT method also to industrial testing purposes.

Requirements on building blocks of the system have also been evaluated and discussed.

REFERENCES

