A 30-mW 10.7-MHz Pseudo-N-Path Sigma-Delta Band-Pass Modulator

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Abstract
This paper presents a sigma-delta modulator designed to convert band-pass signals for digital radio and cellular telephony. The proposed architecture employs only one operational amplifier, thus allowing a reduction of power consumption. A prototype implemented in a 1.2-μm double-poly double-metal BiCMOS technology exhibits an SNR equivalent to 8 bits of resolution over a 200-kHz band, and dissipates only 30 mW with a 5-V supply.

Introduction
Interpolative or band-pass sigma-delta modulation represent the state of the art of A/D conversion of narrow-band signals centred at high frequency. This technique retains most of the advantages of low pass sigma-delta modulators, like inherent linearity, reduced antialiasing filtering requirements and robust analog implementation. Moreover, for quadrature modulated signals the A/D conversion by a single-bit modulator allows a perfectly stable digital demodulation [1].

Band-pass modulators are easy to derive from low-pass ones, by applying the simple low-pass to band-pass transformation $z^{-1} \rightarrow -z^{-2}$. The counterpart is the increased complexity of the modulator compared to the low-pass architecture.

Previous solutions used biquad-based resonators to obtain the required noise and signal transfer functions [2]. This approach requires two amplifiers and one comparator to realise a second order filter function. For higher order modulators a considerably high number of basic elements are needed [3].

The required transfer functions can be implemented using the pseudo-N-path approach [4], thus realising a first-order modulator (i.e. a second-order filtering function) with only one operational amplifiers.

Modulator Architecture
The band-pass modulator architecture is shown in Fig. 1. The oversampling frequency is $f_{os} = 42.8$ MHz, thus allowing the conversion of narrow-band signals centred at $f_m = \frac{1}{4} f_{os} = 10.7$ MHz. Four complementary phases are derived from a master clock at 42.8 MHz by simple division. The resonator transfer function is obtained by a pseudo-N-path architecture (Fig. 1), which implements the complex transfer function with a single amplifier. In this way a considerable reduction of power consumption is obtained. Moreover, all capacitors are integer multiples of a unit capacitor (250 pF in the presented implementation), thus relaxing problems due to intermodulation between signal and clock caused by architecture asymmetries [5].

To evaluate the functionality of the proposed architecture a prototype of the modulator had been realised on a double-poly double-metal 1.2-μm / 7-GHz BiCMOS technology. The basic building blocks are: a high-gain (> 50 dB dc gain) high-speed (350 MHz unity gain frequency) fully-differential operational amplifier and a differential comparator. The area of the modulator is $1.2 \times 0.7$ mm$^2$ and the power consumption is 30 mW at 42.8 MHz clock frequency. Fig. 2 shows the circuit microphotograph.

Experimental Measurements
Fig. 3 shows the analog spectrum of the bit stream at the modulator output. It confirms the functionality of the circuit. The input signal is a 2 Vpp differential sinusoidal tone at 10.68048 MHz, asynchronous with the modulator master clock. Differential voltage references (±1 V relative
to analog ground) are externally supplied to the circuit. Fig. 4 shows an expanded view of the in-band power spectrum.

Fig. 5 shows a digitally evaluated power spectrum, obtained through a Hanning-windowed 65536-point FFT. The estimated SNR over a 200-kHz signal band is larger than 46 dB and corresponds to 8 bits of resolution.

**Conclusion**

This paper has presented a new sigma-delta architecture for the demodulation of high-speed narrow-band signals in telecommunication systems. The pseudo-$N$-path structure allows to implement a second-order filter with only one operational amplifier, thus reducing power consumption. The functionality of the proposed architecture has been demonstrated through a prototype realised and characterised in a 1.2-$\mu$m BiCMOS technology.

**References**


in a 1.2-$\mu$m BiCMOS analog/digital Array,” in *Symp. on VLSI Circ. Digest of Technical Papers*, 1992, pp. 102-103.


