The trend toward higher and wider frequency bands in mobile communication creates the need for high-speed high-resolution data conversion systems. Mobile communication apparatus will have to support either analog cellular services or digital multimedia protocols. Transceiver base stations will be characterized by increasing complexity and flexibility. This can be achieved only by an extensive use of digital processing. For example, Software Radio wants to reduce the hardware front-end to a minimum by digitizing all channels in the cellular band (70MHz) (1). Processing for Software Radio requires resolutions of 10b or more.

This BiCMOS track and hold (T&H) circuit is intended for use as the front end of an A/D conversion system. The T&H operates at 250MHz sampling rate and is capable of limiting the harmonic distortion to -62dB for a 70MHz sinewave input. Similar results are obtained with 10MHz input sinewaves and 200MHz sampling frequency (2). The circuit exhibits hold-mode feedthrough and pedestal errors significantly better than previously-published results. A 12GHz-fs, 0.8um BiCMOS process is used.

The T&H described is the result of known techniques revisited and new ideas. Figure 1 shows the T&H block diagram made up of three sections: input buffer, intermediate switched emitter follower sampler (SEF), and output buffer. The schematic is a single-ended version. The actual circuit is a fully-differential implementation of what is shown in Figure 1, for reduction of second-order non-linearities. The circuit also includes an auxiliary switched emitter follower, whose function will be described later. A bandgap reference and a clock buffer are included in the circuit.

The switched emitter follower concept is proposed by Reference 3. It is based on an emitter follower (Q_em in Figure 1) that, during the hold phase (H), is turned-off because its input is pulled down by the switching-on of Q_em. During the track phase (T) the emitter follower is “on” and transfers the buffered signal to the output. The main concern in this method is proper drive of the switched emitter follower. To avoid ringing in the track phase, it is necessary to use an input buffer with low output impedance (4). This is fulfilled by the use of the input buffer in Figure 2a. Its output resistance is 2R_in and its value is kept to the required low level by a large bias current.

Performance improvements are achieved by clamping the voltage at node A. If, during the hold period, node A drops to uncontrolled levels, the re-charging of the parasitic capacitances associated with node A itself significantly slows down the switching-on. As is seen from the schematic in Figure 1, the problem is avoided by Q_op and the associated circuitry. During the hold phase, since I_H > I_D, Q_op in the input buffer (in Figure 2a) is “off” and the clamping transistor, Q_op, controls the voltage of node A. The voltage of the base of Q_op is V_ba = V_op + V_D. Therefore, node A is clipped at one V_op below V_D. Another function of the clamping circuit is to improve the hold-mode feedthrough. During the hold phase, Q_op establishes a low-impedance path for signals coming through the reversely biased diode Q_op. A hold version of V_op is used instead of the input signal itself leading to superior hold-mode feedthrough reduction (5). The hold capacitance of the auxiliary switched emitter follower is not connected to ground but to the degeneration resistance of the current source I_H. This connection dynamically changes the value of I_H during track mode, bootstrapping the current delivered to the sampling capacitance C_s. The result is that the modulation of V_op is reduced with benefits to the harmonic distortion.

Non-linear contributions of the pedestal error limit accuracy of the circuit. One of the sources of pedestal error is the charge injected by the collector-base junction capacitance (C_j) of the current switches Q_op and Q_em. This contribution is attenuated by two dummy transistors, Q_d1 and Q_d2, driven by complementary phases. They operate as non-linear capacitances and have the floating collectors.

The final output buffer (Figure 2b) drives the capacitance of the following A/D converter (estimated 10pF). Performance of the buffer is improved by a bootstrapping of the collector-emitter resistance of Q_d. The collector of Q_d is biased with the output voltage that tracks the input. The input impedance is thus increased and the droop rate on the sampling capacitance is reduced.

Measurements on the prototype circuit confirm the performance improvement compared to previously-reported circuits. Figure 3 shows the spectrum with 250MHz sampling rate and 70MHz analog input. The input amplitude is 1V_p-p and the achieved harmonic distortion is -61.6dB. Figure 4 shows the degradation of harmonic distortion as a function of the sampling frequency. With 300MHz sampling, the harmonic distortion is -57.3dB. Figure 5 shows measured output in the hold-mode. With an 80MHz and 1 V_p-p input signal the hold-mode feedthrough is -57dB. Table 1 compares the results with the state of the art for similar specifications. All parameters are better, with the exception of slightly larger droop rate resulting from high bias currents.

Figure 6 shows a chip micrograph. It includes two T&Hs for dynamic testing purposes and output buffers. The T&H is 0.5x0.75mm 2 and dissipates 45mA with 5V power supply.

References:


Figure 1: Track and hold schematic.

Figure 2: (a) Input buffers. (b) Output buffers.

Figure 3: Output spectrum with 250MHz sampling rate and 70MHz input sinewave.

Figure 4: Degradation of the harmonic distortion as a function of the sampling rate.

Figure 5: Output spectrum during hold-mode phase with 80MHz, 1 Vpp input sinewave.

Figure 6: See page 444.

Table 1: Measured performance summary and comparison with state of the art.

<table>
<thead>
<tr>
<th>Feature</th>
<th>This circuit</th>
<th>State of the art [2]</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
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<td>20GHz BiCMOS</td>
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<tr>
<td>Droop rate</td>
<td>60μV/νs</td>
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<td>Pedestal error</td>
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<td>8mV</td>
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<td>Harmonic distortion</td>
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<td>-65dB at 10MHz</td>
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<tr>
<td>Hold-mode</td>
<td>feed-through</td>
<td>-57dB at 80MHz</td>
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<td></td>
<td></td>
<td>-52dB at 50MHz</td>
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<tr>
<td>Sampling rate</td>
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<td>200MHz</td>
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</table>
Figure 6: Measured signals for $f_{\text{sample}} = 500\text{MHz}, f_{\text{clk}} = 1\text{GSample/s}$.

Figure 7: Chip comprising two THAs.

Figure 6: Chip micrograph.