A 12 BIT A/D INTERFACE FOR A 3D MAGNETIC SENSOR

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ABSTRACT

This paper presents a high resolution low-power smart system for 3D magnetic field monitoring. The magnetic sensors, integrated on-chip, need a bias current of a few mA to achieve the required resolution. Nevertheless, the proposed 12 bit A/D converter allows pulsed operation of the sensors with a duty cycle as low as 4 \times 10^{-5}, thus keeping the system power consumption below 1 \mu W. The A/D converter operates with 500 kHz clock frequency and achieves a DNL below 0.2 LSB and an INL below 0.5 LSB in worst case simulations. A prototype of the system has been integrated in a 1.2 \mu m CMOS technology.

1. INTRODUCTION

Smart sensors with on-chip A/D interfaces are an essential part of the new generation of microintegrated systems. In order to achieve the best system performance, it is important to select an architecture for the A/D interface which at the same time meets the sensor features and the system requirements. This paper considers an A/D interface for a 3D portable (battery operated) magnetic sensor (magnetodosimeter or magnetic badge), intended for monitoring the exposure of workers to magnetic fields. Several working environments, such as hospitals (magnetic resonance) or physics laboratories (nuclear experiments) are polluted by strong low-frequency magnetic fields. In order to guarantee the workers' health, therefore, it is essential to monitor the exact integral exposure of each worker to a particular level of field. Long exposures to relatively low fields may, indeed, be as dangerous as exposure to a strong magnetic field for a short period of time.

The level of magnetic field which is known to be dangerous for human beings can be detected by silicon magnetic sensors fabricated in conventional CMOS technologies [1]. However, the bias current required to achieve the desired sensitivity (a few mA) is too high to allow battery operation. This potential drawback is circumvented in the proposed system by choosing a particular architecture for the A/D interface, which allows pulsed operation of the sensor with a very small duty cycle. Therefore, despite the large power consumption of the sensors, the average power consumption of the system (sensor and interface) is kept as low as 1 \mu W from a 5 V power supply (with a magnetic field sampling frequency of 1 Hz).

2. SYSTEM DESCRIPTION

The block diagram and the most important specifications of the integrated magnetodosimeter are shown in Fig. 1, and Tab. 1, respectively. The system is based on three magnetic sensors which detect the x, y and z components of the magnetic field in the environment $\vec{B} = (B_x, B_y, B_z)$. The current signals produced by the sensors are multiplexed, transformed into voltages, equalized and converted into the digital domain using a single A/D converter. The resulting words representing $B_x$, $B_y$ and $B_z$ are delivered to the digital section, which calculates the module of the vector and stores the histogram of the magnetic field intensity during the monitored period in a RAM.

![Fig. 1 - Block diagram of the integrated magnetodosimeter](image)

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Consumption (System)</td>
<td>1 \mu W @ 1 Hz, 5 V</td>
</tr>
<tr>
<td>Sampling Frequency of $B$</td>
<td>$1/32$ Hz $\pm$ 1 Hz</td>
</tr>
<tr>
<td>Magnetic Field Range</td>
<td>$-200$ mT $\pm$ 200 mT</td>
</tr>
<tr>
<td>Resolution</td>
<td>100 \mu T</td>
</tr>
<tr>
<td>Memory (1 S/s, 8 h)</td>
<td>4 KByte</td>
</tr>
</tbody>
</table>

Tab. 1 - Specifications of the integrated magnetodosimeter

In order to cover the magnetic field range from $-200$ mT to 200 mT with steps of 100 \mu T (Tab. 1), the A/D converter resolution has to be at least 11 + 1 bits (2048 levels and a sign bit). However, since the sign of the magnetic filed is not relevant in this application, only the 11 least significant bits are stored in the RAM. Hence, the size of the memory required to monitor the magnetic field once per second during a whole working shift is 4 KBytes.

The magnetic sensor used to detect $B_x$ and $B_y$ is a quad-collector lateral magnetotransistor with suppressed sidewall injection (SSIMT). In order to detect magnetic fields in the mT range, this device requires an emitter current of a
few mA [1, 2]. Fig. 2 illustrates the basic structure and the operating principle of a CMOS-compatible SSIMT (only two collectors are shown for simplicity). In the presence of a magnetic field parallel to the chip plane, the carrier deflection, due to the Lorentz force, enhances the current in one collector at the expense of the other. The resulting differences between the collector currents ($\Delta I_{C1,2}$ and $\Delta I_{C3,4}$) are proportional to the corresponding components of the magnetic field ($B_x$ and $B_z$).

![Fig. 2 - Operating principle of a CMOS SSIMT](image)

To detect the $z$-component of the magnetic field, we used a CMOS compatible current-controlled Hall device (CCHD) with one input and three output terminals [3]. The layout and the cross-section of this device are shown in Fig. 3. In order to operate the CCHD with sensitivity in the mT range, a fixed current ($I_{TOT}$) of a few mA is applied to the input terminal ($S_{TOT}$). Moreover, with a second current source, we control the current $I_0 < I_{TOT}$ extracted from the central output terminal ($S_0$). Without an external magnetic field, the residual current $I_{S2} = I_{TOT} - I_0$ is equally divided between the two outer output terminals ($S_1$ and $S_2$). In the presence of a magnetic field ($B_z$) perpendicular to the chip plane, the current in the n-well is deflected due to the Lorentz force acting on the electrons. This leads to a current difference $\Delta I$ between $S_1$ and $S_2$ proportional to $B_z$. Since the sensitivity of the CCHD depends on the ratio between $I_{TOT}$ and $I_0$, we can easily equalize the output signals delivered by the SSIMT and the CCHD, thus allowing a correct detection of the magnetic field module.

![Fig. 3 - Layout and cross-section of the CMOS CCHD](image)

The output currents of the sensors are alternatively connected to a current to voltage converter, i.e., a resistor, by means of an analog multiplexer, as shown in Fig. 4. In order to perform a fine sensitivity and offset calibration, we use three variable resistors and three reference voltages with nominal value of 250 kΩ and 2.5 V, respectively.

![Fig. 4 - Schematic diagram of the multiplexer and current to voltage converter](image)

3. A/D CONVERTER ARCHITECTURE

In light of the large current required to operate the magnetic sensors (4 to 6 mA), we have to keep the sensors active only during a fraction of the acquisition cycle in order to fulfill the power consumption specifications. It is therefore necessary to use a low power sampling A/D converter [4], such as the successive approximation architecture [5] with two-step DAC shown in Fig. 5.

![Fig. 5 - Block diagram of the proposed successive approximation A/D converter](image)

This solution consists of a 5-bit resistive DAC for MSB conversion, a 6-bit binary-weighted capacitive DAC for LSB conversion, a comparator and a Successive Approximation Register (SAR) [6]. In this converter, the input signal is sampled and stored in a capacitive array (the capacitive DAC) at the beginning of each conversion cycle, thus allowing to keep the sensors active only for a few tens of μs. Moreover, since this solution requires only 13 clock per conversion (with clock frequency $f_{ck}$ up to 500 kHz), the delay among the three components of the magnetic field due to multiplexed operation becomes negligible compared to the bandwidth of the considered signals.

The resolution achievable with this approach is, of course, determined by resistor and capacitor matching. In this particular case, 12 bit and 6 bit matching are required in the resistive string (MSBs) and in the capacitive array (LSBs), respectively. The behavioral simulations shown in Fig. 6, performed using the matching parameters of the target technology (Tab. 2), demonstrate that the desired resolution (12 bit) can be achieved with this architecture.

4. A/D CONVERTER IMPLEMENTATION

The complete schematic diagram of the proposed 12 bit A/D converter is shown in Fig. 7. At the beginning of the
conversion cycle, after the sampling and autozero phases, the sign of the input signal is detected by connecting the capacitive array to the analog ground ($V_R$). The obtained sign bit (Sign) is stored and used to determine the value of the resistive string supply voltage, according to

$$V_{R1} = V_R - (-1)^{\text{Sign}} V_{FS},$$  \hspace{1cm} (1)

where $V_{FS}$ denotes the full scale voltage. Moreover, depending on the value of Sign, the output of the comparator is buffered or inverted (XOR).

The conversion of the 5 MSBs ($b_{10}...b_6$, coarse conversion) is performed by connecting the whole capacitive array to the appropriate tap in the resistive string, according to the successive approximation algorithm.

At the end of the coarse conversion, we end up with two adjacent voltage levels in the resistive string which represent the upper and lower approximation of the input signal. By connecting the different capacitors of the capacitive array to one voltage or to the other, we can, then, use the charge redistribution technique to perform the conversion of the 6 LSBs ($b_5...b_0$, fine conversion). After 13 clock cy-

cles, therefore, we obtain the 12 bit digital representation of the input signal at the output of the SAR.

Besides the error introduced by passive component mismatches already considered in the previous section, the accuracy of the A/D converter is also influenced by offset and overdrive recovery of the comparator.

In order to obtain a very low offset comparator, we used the novel autozero/reset scheme illustrated in Fig. 8.

The comparator consists of three stages, namely a gain stage, an offset compensation (auxiliary) stage and an output/reset stage. During the autozero phase ($\Phi_{az}$), the input terminals of the gain stage are shorted, while the offset compensation stage is buffer-connected. The input referred offset voltages of the gain and auxiliary stages ($V_{os,m}$ and $V_{os,a}$, respectively), therefore, give rise to a voltage across capacitor $C_{az}$ given by

$$V_{az} = \frac{A_m}{1 + A_a} V_{os,m} + \frac{A_a}{1 + A_a} V_{os,a},$$  \hspace{1cm} (2)

where $A_m$ and $A_a$ denote the open-loop gains of the gain and offset compensation stages, respectively.

During normal operation ($\Phi_{az}$), then, voltage $V_{az}$, amplified by $A_a$, is subtracted from the output of the gain stage, thus reducing the input referred offset of the comparator ($V_{os,eq}$) to

$$V_{os,eq} = \frac{V_{os,m}}{1 + A_a} + \frac{V_{az,a}}{A_a}.$$  \hspace{1cm} (3)

The schematic diagram of the circuit implementing the gain and auxiliary stages is shown in Fig. 9. It consists of a folded cascode transconductance amplifier with two differential pairs (for the gain and auxiliary inputs, respectively)
and a common output branch.

![Schematic diagram of gain and auxiliary stages](image)

**Fig. 9 - Schematic diagram of gain and auxiliary stages**

In order to overcome the limitations introduced by overdrive recovery, we have to reset the comparator before each decision in the successive approximation algorithm. This task is performed by an output/reset stage, which consists of two analog inverters (with bias current $I_b$) and one digital inverter. During the reset phase ($\Phi_R$), the analog inverters are buffer-connected, thus strongly reducing the gain of the comparator and precharging the parasitic capacitance of the output node to a voltage close to the analog ground (i.e. the threshold voltage of the analog inverter). At the end of the reset phase, the feedback around the analog inverters is opened and the output of the comparator reaches a logic state (high or low) depending only on the sign of the input signal and not on its amplitude.

The most important design parameters of the proposed A/D converter are summarized in Tab. 3. In order to improve the matching between passive components, we used common centroid structures. Moreover, dummy switches and delayed clock phases are used where necessary to reduce charge injection.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unity Capacitor</td>
<td>0.5 pF</td>
</tr>
<tr>
<td>Total Capacitance (64 Units)</td>
<td>32 pF</td>
</tr>
<tr>
<td>Unity Resistor</td>
<td>500 Ω</td>
</tr>
<tr>
<td>Total Resistance (32 Units)</td>
<td>16 kΩ</td>
</tr>
<tr>
<td>Comparator Gain</td>
<td>100 dB</td>
</tr>
</tbody>
</table>

**Tab. 3 - Design parameters of the proposed A/D converter**

5. RESULTS

The proposed system has been integrated in a standard 1.2 μm CMOS technology. A microphotograph of the chip is shown in Fig. 10. The postlayout simulation of the comparator output during a complete conversion cycle with input signal equal to 1 MSB + 1 LSB is shown in Fig. 11. It can be observed that the presence of the reset stage in the comparator allows the desired resolution to be obtained. The integrated prototype is fully functional. It is presently under testing to extract operating features.

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**Fig. 10 - Microphotograph of the test chip**

**Fig. 11 - Postlayout simulation of a conversion cycle with input signal equal to 1 MSB + 1 LSB**

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REFERENCES