A 10.7 MHz Band-Pass Sigma-Delta Modulator in CMOS Technology

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Abstract—The sigma-delta technique for data conversion, after demonstrating as the reference technique for the conversion of low frequency signals, is now becoming more viable in the high frequency field such as wireless IF, digital radio and telecommunication applications. This paper presents practical aspects of the design of a switched-capacitor band-pass sigma-delta modulator in CMOS technology, to be used in digital radio systems. A pseudo-N-path architecture for the design of CMOS band-pass modulator is presented and analyzed. Then the attention is focused on the basic building blocks design. Suitable circuit solutions have been used to obtain the required values for dc gain, gain-bandwidth product and slew-rate. Simulations indicate that the blocks designed allow a fast clock rate suitable for operation in switched-capacitor circuits sampled at 42.8 MHz.

I. INTRODUCTION

Nowadays, the sigma-delta (ΣΔ) technique is a standard in Analog-to-Digital (A/D) conversion for consumer, professional and telecommunication circuits and wireless IF applications. ΣΔ converters are widely used for commercial products, due to their inherent simplicity and to benefits of oversampling and noise-shaping: linearity, simple anti-aliasing filtering and high tolerance to analog component imperfections. By minimizing quantization error in the band of interest and sampling with a high oversampling rate well above the highest input frequency component, it is possible to achieve high Signal-to-Noise Ratio (SNR) and Dynamic Range (DR) by adopting a coarse quantizer followed by digital filter [1].

In recent years, the ΣΔ technique has been extended to the case where the band of interest is centered around a non-zero frequency. One application of these circuits is in digital radio, to convert the intermediate-frequency (IF) signal of superheterodyne radios directly into digital form [2]-[10]. A band-pass ΣΔ modulator requires a very simple digital circuit to demodulate in-phase and quadrature components of the IF signal at one fourth of the oversampling frequency, with no need for a local oscillator nor for a 90° phase shifter. Therefore, a band-pass ΣΔ modulator operated at f_s = 42.8 MHz is suitable for demodulation of signals centered around the intermediate frequency f_0 = 10.7 MHz.

Independently from the frequency of the input signal, the design of high performance ΣΔ converters involves high frequency operation. Satisfying this constraint means analog blocks to be carefully designed. BiCMOS technology has been previously used in the design of high performance modulators, exploiting advantages with respect to CMOS in realizing high-speed analog blocks [11]-[13].

Compared to BiCMOS, the CMOS technology has a great advantage in terms of cost. However it presents some drawbacks, such as the power consumption and the area of the building blocks, which are greater - with equivalent performances - than in the BiCMOS technology.

This paper presents a ΣΔ modulator designed in CMOS technology. The pseudo-N-path technique has been used in the architectural design the modulator, since this approach leads to a design with reduced number of active elements, thus saving power and silicon area.

Suitable circuit solutions have been used in the design of CMOS building blocks (operational amplifier and comparators) to obtain the required values for dc gain, gain-bandwidth product and slew-rate. High-level as well as transistor level simulations of the proposed band-pass converter indicate that the designed circuits can operate with a sampling rate of 42.8 MHz.

II. MODULATOR ARCHITECTURE

The band-pass ΣΔ modulator is derived from the low-pass one, by applying the transformation [14]:

\[ z^{-1} = -\frac{z}{z + 1} \quad (1) \]

This mapping is illustrated in Fig. 1.

By applying (1) to the low-pass integrator, we obtain the band-pass resonator whose transfer function in z-domain is:

\[ H_{\text{res}} = \frac{z^{-2}}{1 + z^{-2}} \quad (2) \]

which corresponds to the time-domain input-output relationship:

\[ x[n] = -x[n - 2] - x[n + 2] \quad (3) \]

From (2), it is apparent that a band-pass ΣΔ modulator re
Fig. 1 - Low-pass to band-pass transformation

quires a filtering block with a second-order transfer function in $\omega$-domain. Using a biquad approach, two operational amplifiers are needed for each resonating cell [2]-[7].

Recently, we presented a circuit which implements the resonator transfer function with only one operational amplifier [13]. The resonator transfer function can be implemented with the pseudo-$X$-path approach, described in [16]. Using this solution, the second-order band-pass $\Sigma$-$\Delta$ modulator requires only one op amp and one comparator, with a significant reduction in area and power consumption.

Fig. 2 shows the switched-capacitor architecture of the complete band-pass modulator and its clocking scheme.

To implement the resonating block described by (3), the modulator must be fully-differential.

The structure is controlled by four phases. Phases 1 and 2 have a time duration $T = \frac{T_c}{2}$, where $T_c$ is the sampling period.

Phases A and B have a time duration $T_c$.

The transfer function is independent of the absolute value of the capacitor $C_\text{r}$, while the resonator gain is controlled by the ratio of $C_\text{in}$ and $C_\text{r}$ or $C_\text{r}$. The designer can choose the most suitable value for $C_\text{r}$ to minimize thermal noise or to release the operational amplifier speed requirements. The output signal is fed back by the 1-bit DAC and the $C_\text{r}$ capacitors.

It is worth noting that the proposed architecture does not require “difficult” capacitance ratios. All capacitors are multiple of a unit capacitance ($C_\text{unit}=0.25 \text{ pF}$ in our design), thus relaxing problems due to intermodulation between signal and clock caused by architecture asymmetries.

III. CMOS BUILDING BLOCKS

A. Operational Amplifier

The design of the operational amplifier requires special care to achieve the required gain, common mode rejection ratio and equivalent input noise.

Fig. 3 shows the schematic diagram of the fully-differential operational amplifier designed. It is based on a folded cascode configuration [17]. The input stage is realized with large NMOS transistors ($W = 1500 \text{ um}$, $L = 1.2 \text{ um}$) in order to achieve the required gain-bandwidth product. To improve high-frequency performance, a capacitive path is provided which is faster than PMOS transistors in the folded branch. A simple common mode feedback circuit, realized by NMOS transistors in triode region, allows control even with a high bias current in the differential stage. Biasing current and reference voltages are chosen so as to optimize bandwidth and dynamics respectively.

B. Comparator

Fig. 4 shows the circuit diagram of the high clock rate comparator. Regeneration is used to reduce power consumption without degrading speed performance [18].
During the amplification phase, the input differential amplifier amplifies the analog input signal, which appears across the collector resistors. During the regenerative phase, the cross-coupled differential pair regenerates the amplified input difference signal. The differential pair controlled by the clock (input nodes clk and clkin in Fig. 4) switches the comparator from the amplification mode into the regeneration mode. When the clock signal is low, the reference current flows through the input amplifier making it active. When comparison is required, the clock signal is made high and the current is switched into the regenerative loop, giving a logic output value.

Load resistors at the drain nodes of the differential stages are split-up into two components. During the amplification phase, the input signal is amplified using the input differential amplifier and two load resistors, to obtain small signal settling with a large bandwidth. During the regeneration phase, two other resistors are added in series to the input load resistors, to increase the gain of the flip-flop. The use of the split-up resistors allows the collector time constant for the amplifier and the flip-flop mode to be reduced. The positive feedback gives a large gain resulting in a high comparator sensitivity.

Finally, two digital inverters were added to the outputs of the comparator to reach the full CMOS output logic levels.

IV. SIMULATION RESULTS

The ΣΔ modulator has been extensively simulated. Behavioral simulations with TOSCA [19] and MATLAB [20] were used to determine the maximum theoretical performance. After the design of building blocks, the whole modulator has been simulated at circuit level in time domain, using SPECTRE simulator. Then the output sequence has been processed to obtain the spectrum of the output bit-stream. The same validation method was previously used for B/CMOS version of the bandpass modulator [12].

Fig. 5 shows the frequency response of the fully-differential operational amplifier. With maximum capacitive load (2 pF applied to each output), the gain-bandwidth product is larger than 380 MHz with a phase margin of about 55°. The dc gain is 56 dB.

With a full-scale input step, the op amp slewing time is less than 3 ns.

The comparator settles to a valid logic value in 4 ns.

Finally, Fig. 6 shows the output spectrum of the modulator, obtained from circuit-level simulation followed by a 2048-point FFT. In the signal bandwidth (200 kHz), the signal-to-noise ratio is better than 46 dB, thus allows us to achieve 8 bits of resolution in the demodulated signal, after low-pass filtering decimation.

The power consumption of the whole modulator is 110 mW. Table I summarizes the main parameters of the designed modulator.
### TABLE I

**Performance Summary of the Band-Pass ΣΔ Modulator**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Frequency</td>
<td>42.8 MHz</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>200 kHz</td>
</tr>
<tr>
<td>Oversampling Ratio</td>
<td>53.5</td>
</tr>
<tr>
<td>Input Signal Range</td>
<td>2 Vpp</td>
</tr>
<tr>
<td>Power Supply Voltage</td>
<td>5 V</td>
</tr>
<tr>
<td>SNR</td>
<td>&gt; 46 dB</td>
</tr>
<tr>
<td>Resolution</td>
<td>8 bit</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>110 mW</td>
</tr>
<tr>
<td>Area</td>
<td>1.1 mm²</td>
</tr>
</tbody>
</table>

Compared with its BiCMOS counterpart [12], the CMOS modulator dissipates more power (110 mW instead of 30 mW) and requires more silicon area (1.1 mm² instead of 0.84 mm²). On the other hand, CMOS technology is less expensive than BiCMOS, so the proposed modulator is very attractive for mixed analog-digital integrated signal processors.

## V. CONCLUSION

This paper has presented the design of a second-order band-pass ΣΔ modulator in CMOS technology. An operational amplifier and a comparator suitable for use inside the band-pass modulator have been designed. The proposed architecture and basic building blocks are suitable for use inside converter structures clocked at 42.8 MHz. Extensive simulations were carried out and results show that the operational amplifier has a bandwidth of 380 MHz while driving a 2 pF load for each output. Simulations carried out on the complete modulator show that its noise floor is as low as 48 dB, corresponding to 8 bits of resolution over a 200 kHz signal bandwidth.

## REFERENCES


