IMPROVING THE LINEARITY IN HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS

Umberto Gatti (M-IEEE)\(^1\), Giuseppe Gazzoli\(^1\), Franco Maloberti (F-IEEE)\(^2\)

\(^1\)Italtel S.p.A.  
Research & Development Center  
20019 Settimo Milanese  
Milano, Italy  
Tel. +39 2 4388241; Fax +39 2 43888593  
E-Mail: umberto.gatti@italtel.it

\(^2\)Department of Electronics  
University of Pavia  
Via Ferrata 1  
27100 Pavia, Italy  
Tel. +39 382 505205; Fax +39 382 505677  
E-Mail: franco@ele.unipv.it

ABSTRACT

Future telecommunication systems will require A/D converters with resolution as high as 12 bit and very high linearity (>90 dB) at more than 40 MHz sampling rate. These specifications make essential the use of digital calibration for attenuating the errors due to analog components inaccuracies. In this paper we propose a correction technique suitable for off-line and on-line operation. For the first approach we use statistical methods and digital look-up tables. For the second one we suggest a system where the input signal is doubly converted: at the required speed and at a reduced rate but with a higher precision. The slow representation updates the calibration digital look-up table while the data of the fast one are corrected by the look-up table itself. Simulations using Matlab on acquired data and extensive system studies indicated more than 15 dB of improvement in the converter linearity.

1. INTRODUCTION

The emerging request of efficiency and flexibility in communication systems leads to architectures where the transmitted and received signal is processed mainly digitally: the conversion to the digital domain must be performed closer and closer to the antenna [1], thus the A/D converter becomes one of the most critical block of new generation transceivers. The A/D converter will be required to work at very fast sampling rates (>40 MHz), with a resolution of 12 bit or more and Spurious Free Dynamic Range, SFDR, better than 90 dBFS. Devices like that are not presently available and new idea must be studied to fulfill future specs.

A possible solution to the above problem is the linearisation techniques for fast A/D architectures proposed in this paper. We discuss two methods: one is for an off-line correction, the second foresees an on-line correction. The first method, requiring only additional digital circuitry, is not capable to compensate ageing and temperature drifts. By contrast, facing ageing effects using on-line methods requires either digital and analog additional circuitry.

2. OFF-LINE CORRECTION

Off-line correction for improving linearity in A/D converter has been proposed in [2]. The method uses a statistic testing technique to measure the real transfer characteristic of the A/D converter; then, the non-linearity information, stored in a digital memory, permits afterwards to correct the output of every fast A/D conversion cycle. The statistical testing uses a training signal with known probability amplitude distribution, usually a sinewave. The produced output codes are processed by means of the Code Density technique [3], [4] to determine the threshold levels of the A/D transfer characteristic. Finally, a suitable look-up table establishes a mapping between the original codes and the ideal ones. With this solution we improve the performances but the achievable accuracy is not better than the A/D original resolution: both inaccurate and accurate codes have the same number of bit. Thus, if for example the used converter has 12 bit, a linearity better than -72 dB cannot be reached.

An improvement in the linearity can be achieved by the solution shown in Fig. 1. Similarly to the method proposed in [2], the system comprises a non-linear N bit converter, a processing system and a not-volatile memory. Again, during the calibration phase, the training signal, sin(\omega t), is sampled, converted with N bit resolution and sent to a the processing block. The codes are analysed with the Code Density technique and the \(2^N\) non-ideal threshold levels, \(V_{tr}^{N}(i)\), are:

\[
V_{tr}^{N}(i) = -A\cos(\pi C(i)/N_l) + V_{off}
\]  

(1)
where $CH(i)$ is the cumulative histogram of $i$-th bins, $N_I$ is the total number of samples taken and $V_{off}$ is the offset voltage.

![Diagram](image)

**Figure 1.** Proposed off-line correction: a) calibration phase; b) normal operation phase

The novelty of our proposal moves from the following observations. To acquire the input samples we use the deterministic sampling, proposed in [5]. While assuring the same precision, the deterministic sampling drastically reduces the number of required samples with respect to random sampling. The key point of this technique is the correlation between the clock signal, $f_{ck}$, the input training signal, $f_{in}$, and the number of signal periods taken, $N_p$. Their relation is expressed by:

$$N_I f_{in} = N_p f_{ck} \quad (2)$$

In order to avoid the duplication of samples with the same amplitude $N_p$ must be a prime number. The number of samples results from the desired accuracy: for a precision of $1/2^M$ LSB, at least $2^M$ samples must be taken for every bin. To assure that $2^M$ samples fall within the least probable bin, $N_I$ must satisfy the following relation:

$$N_I > \pi \cdot 2^M \cdot 2^{N-1} \quad (3)$$

Threshold levels of a 12 bit converter with 0.0625 LSB ($M = 4$) accuracy requires $N_I > 102943$. Thus, the derived centre of the bin can be expressed by a more accurate digital word with $N+M$ bits ($M$ is the improvement). The use of a more precise representation of the centre of bins allows us to linearise the transfer characteristic with an accuracy higher than the data converter resolution, thus improving the SFDR. Of course, it is necessary to use a bigger memory to store the correction data ($2^N$ address, $N+M$ bit words).

### 3. ON-LINE CORRECTION

We will see shortly that the above technique is particularly effective but, being an off-line method, it is not able to take into account variations due to ageing and temperature drifts. Here we discuss an on-line solution capable, as the off-line approach, to map the digital codes at the output of an $A/D$ converter to more precise analog levels. Fig. 2 shows the proposed architecture.

The input signal is converted by the fast main converter, $A/D_1$ while, in parallel a sub-sampled version of the input signal is converted into digital as well with an higher resolution converter $A/D_2$. The system uses an input track-and-hold, T&H$_1$, and eliminates the effect of the skew between CLK$_1$ and CLK$_2$ [6]. The auxiliary branch requires a second high-performance track-and-hold, T&H$_2$, as input interface of the slow and accurate converter. The logic after receiving the two digital representations of the same input sample checks if the correction memory (RAM) properly modify the rough one into the precise one, otherwise, it changes the correction memory by the use of a proper algorithm. If the input is sufficiently busy, all the cells of the memory will be examined within a reasonable interval of time; thus, ageing and temperature drift are compensated. Two RAMs are used for interleaved operations. During one phase, the input signal is used to up-date the data in one of the RAM while the other operates the correction; during the other phase we exchange the role of the two RAMs. With the discussed method, in practice, we map, using the output of $A/D_1$ as addresses of the RAM, the transfer characteristic of $A/D_2$.

Even with this topology it is possible to linearise the transfer characteristic with an accuracy higher than the one of the fast converter. This is achieved in two ways: the number of bit number of $A/D_2$ can be higher than the ones of $A/D_1$; the up-date of the RAM is done by a suitable filtering that "averages" the correction term over many correction samples. Various up-date algorithms has been studied for achieving the best SFDR.

The hardware implementation of the proposed system poses demanding requests for the $A/D_2$ and the T&H$_s$. Fortunately, it is possible to find on the market $A/D$ converters with the required linearity operating up to 2 MHz (enough for our application). For the T&H$_s$ new solutions are necessary. However, the custom realisation presented in [7] showed performances good enough for our application.
Figure 2. Proposed on-line correction: a) RAM1 is active for conversion; b) RAM2 is active for conversion

4. EXPERIMENTAL AND SIMULATION RESULTS

The proposed technique has been analysed either by experimental test (off-line correction) and by Matlab simulation (on-line approach). The written modules for simulation allow to define the A/D converter parameters and to control the input signal generator. The measured spectrum at the output of a commercial 12-bit A/D converter [8] is shown in Fig. 3. We have used a 40 MHz sampling frequency and a 19.00421 MHz input signal (Amplitude = ±12.5 mV). We observe that harmonic components limit the SFDR; in particular we have a strong spurious component (-82 dBFS) at ±1 MHz, resulting from the folding of some harmonic component. Moreover, many other spurious signals exceed -100 dBFS. After the off-line correction, the output spectrum is improved as depicted in Fig. 4. The floor of spurious signals is below -100 dBFS and the worst component is -96.5 dBFS. The achieved improvement of more than 14 dB results from the use of a look-up table with 16-bit resolution.

Figure 3. Measured output spectrum of a commercial 12-bit ADC without correction ($f_{in} = 19.00421$ MHz, $f_{clk} = 40$ MHz, Ampl. = ±12.5 mV)
The off-line method guarantees satisfactory performance over a -20° to 40° temperature range, showing an average linearity improvement of at least 10 dB.

The effectiveness of the algorithm used in the on-line correction results from Figure 6. In this case, a 19.00421 MHz sine wave (Amplitude = ±500 mV) is converted by means of a influenced not ideal 12 A/D converter. Its output spectrum is shown in Fig. 5. Four harmonics appear, the worse at -67 dBFS. We assume the second, 16 bit, converter more precise than the first one; we used for A/D2 a distortion equal to -87 dBFS. We note from Figure 6 that the harmonics are improved of more than 16 dB.

5. REFERENCES


