A LOW VOLTAGE HIGH RESOLUTION PIPELINED INCREMENTAL ADC

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ABSTRACT
A low voltage incremental analog-to-digital converter with a pipelined architecture is presented. Using first order modulators the conversion time is significantly reduced even at low sampling rates while maintaining high resolution. The switched capacitor converter is designed to operate with a 1.8V power supply and uses three pipelined modulators. With careful design and digital correction it is possible to achieve more than 15 bit resolution.

1. INTRODUCTION
Incremental analog-to-digital converters (ADCs) based on sigma-delta modulation have been used for instrumentation and telemetry applications such as contactless angle measurement [1], pressure sensor interface [2], high resolution CCD detector [3] and for signal processing for current mode active pixel sensors [4]. These applications require high resolution and are characterized by d.c. performance such as offset and gain errors, differential and integral nonlinearities [5]. This high resolution entails a slow conversion rate due to the large number of integration cycles required [5, 6] when a first order modulator is used. The conversion time can be decreased by using higher order modulators [5].

The constant reduction of the minimum line width in integrated circuit fabrication implies that lower supply voltages must be used to ensure device reliability. The available external power source may also limit the supply voltage. Increasingly, applications such as biomedical and telecommunications necessitate designs for low voltage supply.

The low-voltage incremental converter presented here is designed to operate at 1.8 V supply and uses a pipeline of first order switched capacitor modulators. With an effective pipeline architecture a relatively fast conversion rate is possible even at high resolutions. The conversion rate is determined by the number of integration cycles of a single stage of the pipeline while the overall resolution depends on the resolution of each stage and the number of pipelined stages.

2. INCREMENTAL ADC
The operating principle of an incremental ADC is very similar to that of a first order oversampling converter with certain differences. The integrator of the incremental converter is reset before each conversion cycle; the input signal is converted at a relatively slow rate - one in every 2^n clock pulses rather than one in every F clock periods, where F is the oversampling ratio multiplied by the Nyquist sampling rate [6]. The digital signal processing required by an oversampling converter usually entails complex digital filtering whereas the incremental converter only needs a counter to retrieve the digital output. The incremental converter operates on a fixed analog data sample whereas the oversampling converter samples continuously the input signal. The incremental converter thus offers simplicity of design, as well as conversion of d.c. signals without dithering [6].

3. OPERATION OF THE CONVERTER
Fig. 1 shows the circuit diagram of the analog section of a first order incremental converter. This section consists of a non-inverting switched capacitor (SC) summing integrator and a clocked comparator. Each conversion cycle consists of 2 phases: the reset phase and the integration phase. During the reset phase, switches S_2, S_4, S_5, S_6, S_9, S_10 and S_12 are closed while S_7 is opened, thus precharging C_1 and C_4 to V_{cm} - V_{dd/2}.

Moreover, operational transconductance amplifiers OTA1 and OTA2 are connected in unity-gain configuration, thus providing input offset compensation for OTA1 and OTA2, by storing the offset inside C_2 and C_3 respectively.

The integration phase is controlled by two main non-overlapping clocks \( \phi_1 \) and \( \phi_2 \). During the \( \phi_1 \) clock, the following operations take place:
(i) S_1 and S_4 are closed and thus the input voltage \( V_{in} \) is sampled on C_1.
(ii) S_11 is closed, thus sampling \( \pm V_{ref} \) on C_4.
(iii) S_9 and S_10 are closed, thus storing the offset of OTA2 on C_3.
During the $\phi_2$ clock, the following operations take place:
(i) $S_2$, $S_3$ and $S_{12}$ are closed such that the value of $(V_{in} \pm V_{ref})$ is integrated into $C_2$.
(ii) $S_8$ is closed thus performing the comparison operation after the input level shift provided by $C_3$. At the end of this phase, the output of the comparator is latched into the D-flipflop.

The integration phase is carried out for $N = 2^k$ times (where $k$ is an integer representing the number of output bits). During the first integration cycle, the output of the comparator is not valid. Therefore, extra control logic is used for $S_{11}$, $S_{12}$ such that $\pm V_{ref}$ is not integrated during the first cycle; the first comparator output is neglected in the computation of the digital word. After $N$ cycles, the digital word is computed as:

$$D = N_1 - N_0$$

and has a maximum value of $(N–1)$, where $N_1$ and $N_0$ represent the number of ones and zeros in the comparator output.

Hence, the integrated value $V_{res}$ is updated in steps of $(V_{in} \pm V_{ref})$ which depend on the previous comparator output. The integrated value $V_{res}(i)$ after the $i^{th}$ cycle is given by:

$$V_{res}(i) = V_{res}(i-1) + \left( V_{in} - (-1 + 2b_{i-1})V_{ref} \right)$$

where $b \in [0,1]$ is the comparator output.

After $N$ integration cycles, the output of the integrator is given by:

$$V_{res}(N) = \left( 2^k V_{in} \frac{C_1}{C_2} - (N_1 - N_0) V_{ref} \right) \frac{C_4}{C_2}$$

The above expression shows that for $k$-bit resolution, $2^k$ integration cycles are required. However, if a number $m$ of first order $k$-bit stages is cascaded into a pipeline architecture, the conversion time will be drastically reduced. This pipeline architecture is built by feeding the residue $V_{res}(2^k)$ from the preceding stage as an input to the successive stage, through a sample and hold (S/H) block which keeps the input constant for the entire conversion process as shown in Fig. 2. As soon as the $V_{res}(2^k)$ of the $n^{th}$ stage has been computed and fed to the S/H of the $(n+1)^{th}$ stage, the $n^{th}$ stage can start processing a new input sample thus achieving a truly pipelined conversion process. A cascade of $m$ first order stages gives a conversion result every $2^{N/m}$ clock cycles with an overall $N$-bit resolution, where $N = km$, thus achieving a speed improvement factor of $2^{N(1-1/m)}$ over the single stage approach. The conversion latency is given by $m(2^{N/m})$ clock cycles.

The digital word of $m$ cascaded stages is given by:

$$V_D = 2^{N/m} (N_1 - N_0)_1 + 2^{N/2m} (N_1 - N_0)_2 + ... + (N_1 - N_0)_m$$

\[ N \]

4. DIGITAL CALIBRATION

Possible sources of error can lead to signals at the input of each pipeline stage to be out of the range of the stage itself. This kind of error can only be corrected by
introducing an attenuation factor, $\alpha$, in each of the first order modulators. This can be achieved by the capacitor ratios $C_1/C_2$ and $C_4/C_2$. Equation (3) is modified as follows:

$$V_D = 2^{N/m} (N_1 - N_0) \frac{2^{N/2m} (N_1 - N_0) \alpha}{\alpha^2} + (N_1 - N_0) \frac{m}{\alpha^2}$$

(4)

This attenuation factor causes a loss in resolution which is given by:

$$\log \left( \frac{1}{\alpha^2} \right) / \log 2$$

(5)

A value of 0.8 is chosen for both capacitor ratios as this gives a loss in the overall resolution of less than one bit as shown in equation (5) above.

The correct value of the residual voltages is achieved using different calibration factors for each stage. Thus the output conversion must be digitally corrected as:

$$V_D = 2^{N/m} \left[ (N_1 - N_0) - O_1 \right] K_1 + 2^{N/2m} \left[ (N_1 - N_0) _2 - O_2 \right] K_2 / \alpha + \left[ (N_1 - N_0) _m - O_m \right] K_m / \alpha^2$$

(6)

where $O_i$ and $K_i$ are the introduced offset and gain factors. The values of these factors depend on the voltage of the reference generator and the capacitance ratios $C_1/C_2$ and $C_4/C_2$.

The digital values of $O_1$ and $K_1$ are determined during a calibration phase at the start-up of the circuit. The calibration phase consists of the following steps:

i) An input of zero is applied to the third stage and the value of the up/down counter $(N_1 - N_0)_3$ will be due to the offset term $O_1$. Then an input of $V_{ref}/2$ is applied and the digital value obtained is stored and the gain error $K_3$ can be deduced.

ii) A zero input is now applied to second stage with stage 3 connected. The digital word is computed including $O_3$ and $K_3$ and is eventually stored. Then $V_{ref}/2$ is applied. $O_2$ and $K_2$ can thus be calculated from the two digital words obtained.

iii) The same procedure is carried out with the two reference voltages now applied to the whole pipeline with stages 2 and 3 already calibrated. Hence $O_1$ and $K_1$ can be deduced.

5. IMPLEMENTATION

5.1 Integrator and Comparator
The system was designed in 0.8um CMOS process and operates at a supply voltage of 1.8V. A Miller OTA is used for both the SC integrator and clocked comparator. The input stage consists of a nMOS differential pair and therefore the input common mode voltage $V_{cm}$ is chosen to be 1.2V in order to ensure that the input transistors have adequate gate overdrive. The value of $V_{cm}$ is chosen to be less than the supply voltage in order to reduce bulk leakage currents through switches $S_3$, $S_4$, $S_6$ and $S_{10}$. The Miller compensation capacitor for OTA2 is connected only when $S_{10}$ is closed and is disconnected during the actual comparison phase: this increases the slew rate of the OTA and hence reduces the comparison time, while still maintaining a low bias current. The clock signal to the D-flip flop is slightly advanced from that of the comparator switches in order to ensure adequate setup and hold times.

The reference voltage can be adjusted by an external resistor. The maximum value of $|V_{in}|$ is given by $|V_{in}| + V_{ref}$ which has a maximum value of $2V_{ref}$. In order to ensure correct operation of the integrator OTA, $V_{ref}$ was chosen to be 0.4V. This maximizes the input dynamic range and accuracy.

5.2 Sample and Hold
The S/H is based on a SC circuit shown in Fig. 3 [7]. During $\phi_1$, since the op-amp is connected in unity gain configuration, the holding capacitor $C_H$ is charged to $V_{in} - V_{cm} - V_{os}$, where $V_{os}$ is the OTA offset. During $\phi_2$, $V_o = V_{in}$ irrespective of the OTA offset. This S/H configuration is compliant with low voltage operation since the common mode input voltage of the OTA is fixed, while still allowing large input voltage swings.

![Fig. 3. Sample and Hold circuit configuration with offset compensation](image)

6. SIMULATION RESULTS
Initial simulation results for a three-stage pipelined converter have been obtained with $V_{dd} = 1.8V$, $V_{ref} = 0.4V$ and a clock period of 5 $\mu$s. The analog output of each first order modulator is sampled
after 32 integration cycles and passed on to the following stage. Thus the pipeline provides a conversion result every 160 µs. Fig. 4 shows typical results for one of the pipelined first order modulators. The analog output $V_{an}$ and the digital word provided by the comparator are plotted for the whole conversion period for $V_{in} = 125$ mV and $V_{ref} = 400$ mV and $\alpha = 0.8$.

Fig. 4. Simulation waveforms for the integrator and the comparator outputs with $V_{in} = 125$ mV, $V_{ref} = 400$ mV and $k = 5$ bits and $\alpha = 0.8$

7. CONCLUSIONS

A switched capacitor incremental ADC for use with a 1.8 V power supply has been presented. The converter uses a pipeline of first order incremental modulators and achieves high resolution with a fast conversion rate. High gain OTAs are used to minimise gain errors; input offset compensation is designed into the comparator and the sample and hold circuit implementations. Digital calibration compensates the residual errors and thus it is possible to achieve a high resolution greater than 15 bits.

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8. REFERENCES


