AN INTEGRATED ALGORITHMIC DIGITAL-TO-ANALOGUE CONVERTER WITH FIR FILTERING

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ABSTRACT

This paper describes the design and integrated circuit (IC) implementation of a new DAFIC (Digital-to-Analogue Filter Converter) using an algorithmic technique for the Digital-to-Analogue (D/A) conversion. Applications of this new building block to analogue echo cancelling and the recovery of digital video signals are also discussed and compared with the traditional solutions.

1. INTRODUCTION

In recent work [1] we have proposed a new mixed mode digital-analogue building block DAFIC (Digital-to-Analogue Filter Converter) capable of implementing the D/A conversion function together with a finite impulse response (FIR) transfer function, as required in many digital signal processing communications systems [2, 3]. The traditional solutions for the implementation of analogue FIR filtering functions are based on the realisation of analogue delay lines that are critically dependent on the non-ideality of the active elements (operational amplifiers or unity-gain buffers) [4, 5]. Alternative passive structures were also proposed based on the operation of switched capacitor (SC) branches with different switching waveforms [6]. However, for long impulse responses these structures are not practical on account of the many switching waveforms required for implementation. In the DAFIC counterpart, the delay line is realised in the digital domain by means of arrays of D-type flip-flops, therefore avoiding the problems of classical solutions.

The Direct-Form implementation of an N-th order DAFIC with M-bit resolution, schematically illustrated in Fig.1, employs N conventional binary-weighted capacitor arrays [7], each with M-bit resolution, to convert and weight the digital word associated with each tap of the delay line. In the alternative architecture with binary-weighted time slot arrays, schematically illustrated in Fig.2, the D/A conversion is realised by means of N simple switched capacitance capacitors, each of which is operated by M switching waveforms organised in a binary-weighted time slot array. While the former architecture requires only two non-overlapping switching waveforms but occupies a large capacitance area, the latter reduces the total amount of silicon area required for implementation at the expense of increased complexity of the switching waveforms and slower speed of conversion.

In order to overcome the problems of the above structures, we introduce in Section 2 a new DAFIC architecture using an algorithmic D/A conversion technique [8]. Section 3 deals with the design and IC implementation of an 8-bit/4-tap algorithmic DAFIC using a 3um double-poly, single-metal CMOS process. Finally, in Section 4 we explore and compare with the traditional solutions the application of DAFIC building blocks to analogue echo-cancelling and video signal processing.

Fig.1-General architecture of an SC DAFIC with direct-form implementation and capacitor array arrangements for the positive and negative impulse response coefficients.

Fig.2-Switching waveforms

2. SC DAFIC ARCHITECTURE USING AN ALGORITHMIC D/A CONVERSION

The new algorithmic DAFIC architecture with M-bit resolution and N-length FIR transfer function is represented in Fig.3. The basic idea behind this structure is the same as in the previous ones, that is, to realise the delay line in the digital domain. However, instead of having the D/A conversion realised at each tap, this function is centralized in the output adder block. This comprises a parasitic and offset-free adder/divider-by-two stage (b) implementing the recursive equation

\[ v_s(i) = \frac{1}{2} \left( v_s(i-1) - \frac{Q_t}{C_p} \right) \quad \ldots (1) \]

where \( Q_t \) is the charge injected through the virtual ground in each time slot. Therefore, the delayed digital words are passed bit-by-bit to the output block by means of appropriate shift registers, and weighted according to the corresponding transfer function coefficient \( h_m \) (\( m=0 \ldots N-1 \)). For clarity of
Fig. 3-2a SC DAFIC architecture with binary weighted time slot arrays, and switch arrangements for b) positive and c) negative impulse response coefficients.
d) Example of phases A0, A1, A2 and A3 for n=4

exp anation, let us consider only the tap corresponding to bnx0 (Fig. 3-3b) connected to the output block, and the switching waveforms of Fig. 3-3d. At the end of the resetting slot (θR) and its complement, we have at the output

\[ V_s^b(1) = \frac{C_n}{C_p} b_n V_s \]  

(2)
even if the OA has a non-zero offset voltage \( V_{OS} \). At the end of the next time slot we can write

\[ V_s^b(2) = \frac{C_P}{C_P + C_r} V_s^b(1) + \frac{C_r}{C_P + C_r} b_n V_s \]  

(3)
If the two feedback capacitors are precisely matched, \( C_P = C_r \) then expression (3) can be written as

\[ V_s^b(2) = \left( V_s^b(1) + \frac{C_r}{C_r} b_n V_s \right) \frac{1}{2} \]  

(4)
By computing equation (4) \( W \) times, we obtain at the end of the \( W^{th} \) time slot

\[ V_s^b(2) = V_s^b(W) = \frac{C_r}{C_r} V_s \sum_{n=0}^{W-1} b_n 2^{-n} \]  

(5)
This means that the digital word associated with the \( n^{th} \) stage is converted and weighted by \( C_r/C_P \). Considering now the contribution of all the \( N \) taps, and by using the result in (6), we find that the total output voltage conversion level is

\[ V_s^b(2) = \frac{C_r}{C_r} V_s \sum_{n=0}^{N-1} \sum_{k=0}^{n} b_k 2^{-k} \]  

(6)
The sign that must be considered for each tap is defined by the switching waveforms that control the switching associated with the corresponding capacitor, as shown in Fig. 3-3b and 3-3c, respectively, for \( h_n > 0 \) and \( h_n < 0 \). In order to preserve the DC gain of the FIR transfer function the condition

\[ V_{max}^b = V_s (1-2^{-N}) \sum_{n=0}^{N-1} b_n \]  

(7)
must hold for the full scale output voltage conversion level (all bits at high-level). By using (6) and equating for \( V_s^b \) we obtain

\[ C_n = \left| h_n \right| C_r \]  

(8)
yielding

The correct operation of the algorithmic DAFIC architecture is based on the precision of switching waveforms \( \Phi_0, \Phi_1 \) and \( \Phi_2 \) (Fig. 3-3d) and the matching between the two feedback capacitors \( C_P \) and \( C_r \). In Table 1 we summarize some of the more important characteristics of this DAFIC architecture, and compare them with those of the previously proposed architectures. This leads to the conclusion that the algorithmic DAFIC gives the best compromise between speed of conversion, accuracy and area occupied, and surely is particularly suitable for IC implementation.

<table>
<thead>
<tr>
<th>DAFIC ARCHITECTURE</th>
<th>DIRECT-DOM</th>
<th>BINARY-WEIGHTED TIME SLOT ARRAYS</th>
<th>ALGORITHMIC</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W ) SWITCHES, WAVEFORMS</td>
<td>2</td>
<td>( W )</td>
<td>3</td>
</tr>
<tr>
<td>TIME OF CONVERSION (TIME SLICES)</td>
<td>1</td>
<td>( 2^W )</td>
<td>( W )</td>
</tr>
<tr>
<td>CAPAC. AREA (DC GA)(%)</td>
<td>( W ) ( .2 )</td>
<td>( W ) ( .2 )</td>
<td>3C</td>
</tr>
<tr>
<td>CAPAC. SPREAD (DC GA)(%)</td>
<td>( W ) ( N )</td>
<td>( W ) ( N )</td>
<td>( N )</td>
</tr>
<tr>
<td>MATCHING REQUIREMENTS</td>
<td>( C_n = 2C_{n-1} )</td>
<td>( C_r = C_P )</td>
<td></td>
</tr>
</tbody>
</table>

Table 1: Comparison of DAFIC architectures.

3. INTEGRATED CIRCUIT IMPLEMENTATION

**Analog Circuit Components**

In SC circuits, the fact of having only purely capacitive loads enables the utilisation of high output impedance operational amplifiers (OA's) which do not need a special output buffer stage. Besides, with CMOS technology it is possible to design single stage OA's with a gain sufficiently high for operating in SC circuits. Therefore we have selected for the implementation of the algorithmic DAFIC
described above an OA employing the folded cascade structure shown in Fig.4. The compensation scheme of this OA is achieved by its own capacitive load. The (N/1) aspect ratios of the transistors were designed for 70 dB DC-gain, 7 MHz of gain-bandwidth product and 250ns settling time. The resulting power consumption is only 670µW for 5 V power supply.

The analogue switching employed in this DAFIC are simple CMOS transmission gates. However, since in this circuit the switches are always coupled in pairs with a common node, as shown in Fig.5a, we have implemented the cell as it can be seen in Fig. 5b. This leads to a more compact layout.

Digital Shift-Register Cell

Since the frequency of the shift-register cells is 4 times faster than the frequency of conversion, and since this is, in many cases, of the order of tenths of kHz, we decided to implement the shift-registers using the basic dynamic cells shown in Fig.6. The switches are also CMOS transmission gates as in the analogue case, and the inverters are minimum dimension CMOS inverters, as it is represented in Fig.7. The W-bit shift registers necessary for the DAFIC implementation are built by the serial connection of W basic shift register cells. At the end of each shift register, the interface between the digital circuit and the analogue part is realised by the configuration shown in Fig.8.

Chip Planning and Layout

Integrated circuit performances may be seriously affected if the layout does not receive some care.\cite{9} As the case of the present DAFIC building block, noise injection via the substrate, latch-up problems, bad power supply rejection ratio, sensitivity to process variations, bad component matching, high offset voltages due to asymmetry in components, high parasitic capacitances and excessive clock feedthrough are some of the problems that may be raised by a careless layout. Some layout techniques were developed in order to avoid this kind of problems and to assure that the integrated circuit will work as perfectly as possible. In the layout of the operational amplifier, illustrated in Fig.9, the MOS transistors were implemented in an interleaved form (stacked implementation) in order to guarantee a good symmetry. Similarly, we can see in Fig.10 the capacitor block comprising many unit capacitors interconnected in an interleaved form. These correspond to the two feedback capacitors C_f and C_w that must be very well matched. From another standpoint, to ensure that the analogue section is shielded against the noisy spikes generated by the digital circuitry, we have utilised two layout techniques. The first consists of separating the power supplies of the two sections, while in the second we bias the substrate under the analogue circuitry with an involving guard ring connected to the analogue VDD. This technique maintains the inner substrate at a nearly constant potential free of spurious spikes, and minimises the noise transmission via the substrate. This technique is visible in the floor plan of the chip presented in Fig.11, where we can see the two distinct sections. The total silicon area occupied is 1.5 mm² (PAD's included) and the total DC power consumption estimated is less than 1mA for a 5-V power supply.
4. APPLICATIONS OF THE SC DAFIC BUILDING-BLOCK

In this section we present and discuss two possible applications where the DAFIC building block seems to be a good alternative to the classical solutions.

Analogue Echo Cancelling Architectures:

Fig. 12 shows a typical hybrid-based architecture [10, 11] where echo cancellation techniques are used in order to compensate for hybrid unbalance and therefore improve the separation between the transmit and receive signals. The echo canceller is essentially an adaptive transversal filter [11] where the tap coefficients are modified such that its output may be a good replica of the echo of the transmitted signal through the hybrid and into the receiving path. Different approaches are adopted for the subtraction of the echo estimation from the received signal, depending whether it is made in the digital or in the analogue domain, or even if the filter is analogue or digital. Since the DAFIC realises a transversal filter in a mixed digital-analogue mode, it can be used in echo cancellation applications if we make it programmable. Fig. 13 shows a possible configuration for an echo cancellation system using a programmable DAFIC architecture. Programmability of the DAFIC can be assured if we associate to each delay stage a programmable capacitor array instead of a single capacitor. Notice that for changing the sign of each tap coefficient, it is enough to interchange the switching waveforms that control the switches associated to the corresponding capacitor, as we have shown in Fig s 3-b and 3-c.
**Video-Signal Recovery Applications:**

The traditional solutions for the recovery of digital video signal always require FIR filtering in order to ensure a constant group-delay characteristic. In Fig. 14-a we present a typical scheme for the recovery of digital video signals. On this case, the application of the DAPIC building block is straightforward and does not require any special adjustment, as it is shown in Fig. 14-b.

![Diagram](image)

Fig. 14-a: Traditional solution for recovery of digital video signals.

Fig. 14-b: Alternative architecture using an DAC.

**5. CONCLUSIONS**

In this paper we have introduced a new DAPIC architecture which utilizes an algorithmic D/A conversion technique. This solution gives a better compromise between accuracy, conversion speed and silicon area than on previously proposed architectures. A design example and corresponding IC implementation was given of an 8-bit/4-tap algorithmic DAPIC. The application of DAPIC building blocks to analogue echo cancelling and the recovery of digital video signals was also discussed with a view to obtain improved design solutions and circuit performance in comparison with traditional solutions and circuits.

**References**


