Abstract

This paper relies on the design of an high-performance Track-and-Hold, intended to be used in data converters for telecommunication applications. Because of the challenging performance requirements an advanced SiGe bipolar technology ($f_T = 75$ GHz) has been used to implement the circuit. T&H measurements show a third harmonic better than -87 dBFS with a 1 Vpp,diff input level, 110 MHz – 1kHz signal frequency, and 110 MHz clock rate. Current consumption is 25 mA @ 5 V supply (not including the low-jitter clock buffer). The other performance are at the state-of-the-art.

1. Introduction

Wide-band (multi-channel) IF-sampling base-stations provide challenging specifications for Analog-to-Digital converters and the associated input Track-&-Hold. They require excellent performance in terms of signal range and noise (SNR), Harmonic Distortion (HD) and Spurious Free Dynamic Range (SFDR), and clock rate, all over a wide bandwidth at an intermediate frequency between 50 and 100 MHz. One of the bottlenecks to the implementation is the input T&H. Typical requisites for this block are the following: clock rate and input signal frequencies of about 100 MHz (signal bandwidths from 10 MHz to 25 MHz), harmonic distortion below -86 dBFS (mainly the 3rd) and noise floor below 2 nV/sqrt(Hz).

SiGe is the enabling technology for this class of circuits. With respect to silicon only technologies it offers reduced transit time (1.2 ps) and junction capacitances, lower base spread resistance, and higher Beta and Early voltages. All these advantages impact positively on the speed, noise, linearity and consumption performance of the T&H.

This paper presents a T&H integrated with an advanced BiCMOS SiGe process (the CMOS option is not used in this implementation). It provides NPN transistors with $f_T = 75$ GHz, vertical PNPs with $f_T = 6$ GHz (all at Vcb=0), and MOS capacitors with 3 fF/mm² (apart LPNPs, MIM capacitors, varactors, inductors and different types of resistors). A third harmonic of -87 dBFS is achieved at a 1 Vpp,diff input level, 110 MHz – 1kHz signal frequency, and 110 MHz clock rate (the second harmonic is at -76 dBFS). Current consumption is 25 mA at a 5 V supply (not including the low-jitter clock buffer). This T&H outperforms previous realisations, like the ones described in [1] and [2].

2. Track-And-Hold design

The T&H architecture is similar to the one reported in [3]: it uses an input buffer, a Switched Emitter Follower (SEF), and an output buffer. The previous solution achieved more than 60 dB SFDR with 250 MHz sampling frequency. The result is remarkable; nevertheless, for modern applications more than speed it is necessary to achieve excellent SFDR performances. Significant enhancements have been introduced in the new version mainly to improve the overall distortion behavior. In particular, the technology used makes available high speed pnp transistors. Therefore, we have replaced the P-MOS current generators with more linear bipolar counterparts. Moreover, as discussed below, we made a number of improvement either at the circuit level and at the layout level.
Fig. 1 shows the schematic diagram of the input buffer and sampler in a differential arrangement. In the track phase $Q_{s1}$ is on, $Q_{s2}$ and the clamping transistor $Q_{clp}$ are off, and the buffered voltage is loaded into the sampling capacitor, $C_s$. While feeding the hold capacitor, an auxiliary signal path compensates for the $V_{be}$ modulation of $Q_{out}$, by counter modulating the bias current. This is achieved with the auxiliary SEF and capacitor $C_{s'}$, equal to $C_s$ in magnitude, connected to the common emitter of $Q_{s1}$ and $Q_{s2}$. The harmonic distortion at the end of the track phase is largely reduced with this mechanism, together with the high-speed performance of the SiGe technology used. In the hold phase, the SEF bias current is switched from $Q_{s1}$ to $Q_{s2}$ and, since $I_b > I_{b1}$, the diode $Q_3$ turns off and $Q_{clp}$ turns on. This isolates the hold capacitor from the input. In order to guarantee an approximately constant pedestal error from sample to sample, the auxiliary SEF is also used to generate the voltage applied to the base of the clamping transistor. The local-feedback in the input buffer [4] provides a wide bandwidth together with a reduced output impedance ($2/g_{m,in}$). Vertical PNPs have been used in the sourcing current generators, as well as in the level-shifters of the auxiliary SEF.

Dummy switches $Q_{dm1}$ and $Q_{dm2}$, with shorted base-emitter junctions, have been added to minimise the pedestal error. As they are driven with opposite phases with respect to the correspondent main switches, a compensation is achieved for charge injection through the non linear and matched parasitic capacitance $C_{bc}$ of $Q_{s1}$ and $Q_{s2}$.

Rejection of hold-mode feed-through is achieved with the low impedance path created by the emitter of the clamping transistor, $Q_{clp}$. Further reduction is achieved via the cross-connected capacitors, $C_{ff}$, built with a series-parallel connection of four diodes [5]. Fig. 2 shows the output buffer. With respect to the buffer used in the input section, a final level-shifter has been added to drive the foreseen load. As base current impacts on the droop rate, a compensation circuit has been added. Transistors $Q_{m1}$ and $Q_{m2}$ mirror the base current in $Q_4$ and inject it in the base of $Q_1$. Since the base current of $Q_4$ ideally equates that of $Q1$ a minimisation of the common-mode voltage droop is achieved.

**Figure 1.** Schematic diagram of the track-and-hold circuit

**Figure 2.** Output buffer
3. Measurement results

The track-and-hold was designed using the above-mentioned SiGe technology. A micrograph of the chip is shown in Fig. 3. The overall chip area is 1.3x0.9 mm$^2$ and is packaged in a 28-pin TSSOP. Each die includes two cascaded T&Hs (each with 0.4x0.25 mm$^2$), and a low-jitter clock buffer. The second T&H has been included for testing purposes. Its function is to re-sample the output of the first T&H at the end of the hold phase [5]. The schematic diagram of test setup used together with the timing waveforms is shown in Fig. 4. Both T&Hs are sampled at the same rate with non-overlapping clocks. The clock input to the IC is a sinusoidal low phase-noise oscillator, which is then squared internally via a low noise amplifier. The input signal is filtered to obtain a pure tone and transformed from single-ended to differential by means of a balun [6]. Fig. 5 shows the measured output spectrum with at 110 MHz clock rate, and a 110 MHz – 1kHz and 1 Vpp differential analog input. Under these test conditions a signal at 1 kHz appears at the output (the x-axis is expressed in bins. Bin 263 corresponds to the 1 kHz fundamental). The third harmonic is at a –87 dBFS level, while the second harmonic is at –76 dBFS. A fully differential scheme should show only odd harmonics. In our case we have a second harmonic component because of mismatches between the differential branches in the input balun and into the ATE measurement instrumentation. The two spur tones nearby the fundamental as well as the increased noise floor are due to the signal generator itself [7], as they are not rejected by the bandpass filter. Moreover, we have the contribution from the jitter of the clock generator.

![Figure 3. Die micrograph](image)

![Figure 4. Re-sample measurement set-up](image)

![Figure 5. Output spectrum (Blackman-Harris window) with 110 MHz sampling rate, 1 Vpp,diff and 110 MHz – 1kHz MHz input sinewave](image)

The spectrum in Fig. 5 results from the following post-processing: the 1 kHz signal is filtered with a 100 kHz bandwidth filter followed by a 10 kHz filter at the input of the acquisition channel. Then, we have a 125 kHz 16 bit 1
V_{FS} A/D converter. Around the bin #1000 (approximately 4 kHz) the spectrum is 5 dB higher than what we have at high frequency. Therefore, the noise of the T&H is 5 dB more than the one of the 16 bit converter clocked at 125 kHz. This permitted us to calculate indirectly the noise spectrum: it is approximately 50 nV/√Hz.

Fig. 6 shows the behavior of the 3rd harmonic as a function of the level of the input signal. The signal voltage ranges from 0.4 to 1.6 V_{pp,diff}. Result shows that for 1 V input the HD\textsubscript{3} is -78 dBFS and changes almost linearly from 0.5 V to 1.5 V with a slope of 6 dB/oct. The measured hold-mode feed-through, with experimental conditions equal to the ones used for Fig. 5, is less than -100 dBFS for a single T&H. Table I summarises the measured performance which confirm the improvement in comparison to previously-reported circuits.

![Figure 6. Degradation of the third harmonic as a function of the differential input signal amplitude](image)

Table I: Summary of T&H performance

<table>
<thead>
<tr>
<th>Feature</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>Bipolar SiGe (f\textsubscript{T} = 75 GHz)</td>
</tr>
<tr>
<td>HD\textsubscript{3} (1 V_{pp,diff}@110 MHz)</td>
<td>-87 dBFS</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>110 MHz</td>
</tr>
<tr>
<td>Hold-mode feedthrough</td>
<td>&lt; -100 dBFS</td>
</tr>
<tr>
<td>(1 V_{pp,diff}@110 MHz)</td>
<td></td>
</tr>
<tr>
<td>Input Equivalent Noise (simul.)</td>
<td>&lt; 6 nV/√Hz</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>125 mW (@5 V)</td>
</tr>
</tbody>
</table>

Observe that the achieved HD\textsubscript{3} is for 110 MHz input sinusoidal wave. This permits to achieve 14 bits of resolution within the full Nyquist band for 110 MHz clock. Moreover, the total power consumption is as low as 125 mW @ 5V supply voltage.

4. Conclusions

In this paper we have presented a Track-&-Hold circuit implemented in an advanced SiGe bipolar technology. The proposed architecture is a revisiting of an already presented architecture [3] that exploits the peculiarity of the advanced process used. The achieved results show that the linearity performance and power consumption significantly benefits of the SiGe low parasitic capacitance and speed. Moreover, circuit improvements and better clock feedthrough compensations lead to measure a third order distortion better than -87 dBFS. The result was reached with input signal with 1 V_{pp,diff} amplitude and frequency of 110 MHz. Moreover, the proposed T&H is able to keep an equivalent resolution better than 12 bit even when the input signal goes up to 1.6 V_{pp,diff}.

5. Acknowledgments

The authors wish to thank Dr. Sara Mazzoleni and Dr. Roberto Scotti at Italtel Quality Department. Work supported (in part) by the E.C., SMT Programme, project DYNAD. Dr. Dias is in a sabbatical leave from IST, Lisbon, Portugal.

6. References

[7] Rhode&Schwartz Signal Generator SMPC.