USE OF A 90° PHASE SHIFT DETECTOR AND SAMPLED-DATA LOOP FILTER IN PLL

Joohwan Park, Franco Maloberti*

Department of Electrical Engineering
Texas A&M University, College Station, Texas, USA
jhpark@ee.tamu.edu
(*) Department of Electronics
University of Pavia, Italy

ABSTRACT

A modified architecture of a PLL that permits a fully monolithic integration is proposed. The key features of the architecture are the use of a phase frequency detector (PFD) operating on a 90° phase shift and a switched capacitor filter instead of a passive filter. The PFD operates with relatively long current pulses, thus reducing non-ideality with respect to the conventional PFD. A behavioral model in Matlab-Simulink has been used for different PFD and low pass filter (LPF) used in the proposed architecture. Results show that the proposed solution achieves the same performances of a conventional solution with 11 times less capacitance.

1. INTRODUCTION

Phase-locked loops (PLL) are important blocks for RF system designs. The PLL is used for many radio applications including frequency synthesizers, frequency multipliers, modulator and demodulator. The prevailing requirements for communication systems are, at the same time, high-quality and low price. In particular, the use of a PLL in many transceivers must comply with the request of frequency hopping. Therefore, we need a well-designed frequency synthesizer in both transmitting and receiving paths to quickly settle to the new required frequencies. The designer achieves small size and low cost targets only if the PLL is fully integrated on-chip with all the necessary components. Unfortunately, in conventional solution, the filtering request for the low-pass filter imposes the use of external capacitors or demands for large silicon area that, in turn, increases the cost. In order to minimize costs and preserve performances this paper proposes a new approach based on the use of a 90° phase shift detector and a switched-capacitor loop filter. The solution has some benefit with respect to the conventional architecture and facilitates a fully integrated approach.

2. BACKGROUND ELEMENTS

The basic building blocks for the frequency synthesizer are the PFD, the low pass filter (LPF), a voltage controlled oscillator (VCO) and a divider. The divider value sets the frequency that the PLL must synthesize. Key design issues concern the tradeoff between the loop filter bandwidth and settling time, and VCO noise suppression by the feedback loop. To get fine tuning in the PLL output frequency without serious fractional spur, it is necessary to randomize the choice of the modulus with sigma-delta modulation [1], so that the average divider ratio is still equal to the desired value but individual division factors occur only for short periods of time.

The above technique in effect converts the systematic fractional sidebands into random noise. Therefore, each PLL block must be designed to achieve fast settling time and low phase noise.

The operation of the PLL relies on the integration of sharp complementary current pulses, whose high frequency components must be filtered out carefully. The time constants of the loop filter require the use of a continuous time passive or active filter which capacitor values are too large for monolithic integration.

3. MODELING A CONVENTIONAL PLL

The comparison of a conventional PLL and the new solution proposed here requires a suitable behavioral description of the elementary blocks. The Matlab-Simulink

Fig. 1 - General PLL block diagram
environment permits us to achieve the goal.

Fig. 1 shows the general block diagram of a PLL. The feedback loop causes the two input signals at the input of the PFD to lock, so the VCO output frequency is the fraction multiple of input frequency. The synthesizer output frequency is determined by the divider factor, that is N or N+1 depending on the control of the sigma-delta modulator.

A feeling of the behavioral models used is provided by Fig. 2 [2]. It shows the behavioral model of the PFD and represents the three state PFD widely used because of its wide linear range and ability to capture phase and frequency. The circuit consists of two edge-triggered D flip-flops. The PFD detects the phase and frequency difference between the two input signals. The 0° phase shift lock has two D flip-flops with reset.

![Fig. 2 - Conventional PFD](image)

Fig. 3 shows the third order, type-2 charge-pump PLL with a passive filter. It is a critical element in the real circuit design, owing to the finite rise-time and fall-time resulting from the capacitance [3]. The pulse may not have enough time to reach a logical high level, failing to turn on the charge pump switches when the phase difference is minute (Fig. 4). Also, when the frequency detector misses the rising edge by high noise, it causes an incorrect charge injection to LPF. All the above mentioned non-idealities are modeled in our behavioral description.

![Fig. 3 - Charge pump PLL structure](image)

4. PROPOSED PLL ARCHITECTURE

The signal at the output of the charge pump is a sequence of current pulses that are transformed into voltage by the loop filter. Therefore, we have an elementary sampled data action (achieved with the charge pump) that is translated into a continuous time output. The basic idea of the solution proposed here counts in enriching the signal processing in the sampled-data domain before moving into the continuous-time. To do this, it is necessary to have at the output of the charge pump a sampled data signal that can be processed by a switched capacitor network. Fig. 5 shows the structure that permits to satisfy the request.

The current of the generators controlled by the PFD is integrated on the capacitor $C_s$. During phase 2 the charge is transferred to a switched capacitor network. Then, the switch 1 resets $C_s$ during the phase 1. A conventional PFD switches on one of the current generator for a very short time. The voltage across the capacitor $C_s$ is the integration of the pulse current. As already mentioned, the noise on the rise and fall time of the current pulse affect the accuracy of the integration.

![Fig. 5 - Switched capacitor charge pump](image)

![Fig. 6 - Proposed PFD/Charge pump output waveform](image)
In order to avoid the limit of the phase lock operation, the PFD switches sequentially the upper current generator and the lower one by almost 90° of the input period. A 90° phase shift lock produces bipolar pulses that are long enough to make the rise on and off transients negligible (Fig. 6). It turns out that above strategy permits us to avoid the gain loss that occurs in the conventional PFD for phase shifts that are close to zero degree.

The reset of the sampled data signal implies the use of a switched capacitor filter, thereby allowing a significant reduction of the total capacitance required for the active implementation. However, the condition established by the $kT/C$ noise must be verified. The capacitor $C_s$ can be eventually used as the input element of a switched capacitor filter (Fig. 7).

![Fig. 7 - Proposed PFD and SC filter](image)

5. BEHAVIORAL SIMULATION

The conventional architecture and the switched capacitor based solution (with 0° phase shift and 90° phase shift) have been compared using behavioral simulations. The basic blocks used account for the following non-idealities:
- noise on the VCO input
- jitter on the reference frequency
- thermal noise in the loop filter

Fig. 8 shows the high level schematic of the VCO in the Simulink environment. The noise is injected in the Mux block and the function Fcn accounts for a non-linear transformation of the two inputs into a frequency controlled square wave. The behavioral simulation permitted us to extensively study the response of the PLL architectures. Namely it is possible to study the transient response and to estimate the phase noise (PN) at different frequencies [4], [5].

![Fig. 8 - VCO block with phase noise in Matlab-Simulink](image)

6. SIMULATION RESULTS AND COMPARISON

Here we discuss the results of behavioral simulations on the conventional and the switched capacitor based architecture. The most critical design point concerns the optimization of the switched capacitor loop filter and the smoothing block (see Fig. 7). The switched capacitor filter has been designed using the bilinear transformation of the continuous-time counterpart. The smooth filter is a single pole low pass with its -3 dB at 1/12 the clock frequency of the SC network. Moreover, behavioral simulations permitted to optimize the transient response of the SC version. A relatively limited modification of capacitor values made the transient response of the continuous time and the SC architectures almost equal.

Fig. 9 shows the SC loop filter. The optimized capacitor values are given in Table 1. Fig. 10 and Fig. 11 show the output spectrum with jitter and with VCO noise for the conventional and the SC architecture.

![Fig. 9 - Switched capacitor filter](image)

![Fig. 10 - Conventional PLL output frequency response (a) with input jitter (b) with VCO noise](image)
The effect of the jitter on the two solutions is significantly different far away from the center frequency (128.3 MHz). The SC version shows a phase noise that goes down to −200 dB at a 50 MHz distance. Moreover, the phase noise at 50 KHz of the SC version is more than 3 dB better than the CT solution.

Also the noise at the input of the VCO affects differently the two architectures. The continuous-time or the sampled-data feedback influences differently the noise at the input of the VCO. The frequency behavior of the loop filter must smooth the phase error every clock cycle and, at the same time, generate corrections opposite to the noise behavior. Also, it is necessary to comply with the requests of frequency hopping which depends on the loop bandwidth and other parameters.

As far as the above points are concerned, the proposed switched capacitor version is favorable: it foresees a reset of the capacitor that integrates the signal charge every clock period. Therefore, it can be as large as required to decrease the phase noise. By contrast, a large capacitor at the input of a conventional PLL causes slow locking time and slow recovery time against the VCO phase noise.

In order to have comparable architectures, the results of Fig. 10(b) and Fig. 11(b) refer to the same value of input capacitance. Therefore, both curves show an almost equal noise floor. However the phase noise at 10 kHz and 50 kHz of the SC version is better than the conventional counterpart by 2 dB and 8 dB respectively.

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<th>Conventional</th>
<th>Switched Capacitor</th>
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<tr>
<td>$R_C$</td>
<td>100 KΩ</td>
<td>1 pF</td>
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<tr>
<td>$C_1$</td>
<td>300 pF</td>
<td>17 pF</td>
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<tr>
<td>$C_2$</td>
<td>30 pF</td>
<td>1.7 pF</td>
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Finally, as shown by Table 1, the value of capacitors required is significantly less for the SC architecture. The SC network requires around 30 pF (including the smooth filter) while the conventional solution requires 330 pF.

7. CONCLUSIONS

In this paper, we have described a new architecture of phase locked loop and verified its operation with a behavioral model description in Matlab-Simulink. The results are compared with a conventional PLL model based on a 0° phase shift PF and charge pump structure. Furthermore, the proposed solution modifies the 0° phase shift PF into a 90° phase shift PF to be used together with a sampled data switch capacitor filter. The approach makes feasible a fully integrated implementation. The only drawback is a slight increase of the power consumption. Moreover, the 90° phase shift PLL doesn't need to use flip-flops in the PF, which can lead to some noise while they identify the transition times. Also, the use of the reset typical of the switched capacitor loop filter provides significant advantages in the chip area and error such as missing edge detection.

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REFERENCES


