JFET-CMOS MICROSTRIP FRONT-END

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While the CMOS version of the front-end chip developed for the microstrip vertex detector of the Aleph experiment is ready to go into operation, a new development is being carried out to achieve a reduction in noise. The improvement is related to the use of a JFET-CMOS chip design which is described in the present paper.

1. Introduction

A multichannel front-end chip has been developed for the microstrip signal processing in the vertex detector of the Aleph experiment. Each acquisition and processing channel consists of a charge-sensitive preamplifier with a dynamic reset of the feedback capacitor followed by a switched-capacitor sampled-data shaper. The shaper realizes a discrete-time triangular weighting function, which would approach the best estimate of the detector charge if only white noise was present, and stores the analog information at the measurement instant. The values stored in all the acquisition channels can be multiplexed upon command onto an output line and taken out of the chip serially [1,2].

The present version of the chip is based on a CMOS process with 3.5 μm gate length. The input device in the preamplifier is an N-channel MOSFET with a gate width W of 1000 μm, which would provide a capacitively matched operation with a 3 pF detector. The actual microstrip capacitance is larger than 10 pF, so that a mismatched operation will occur. Exact matching, on the other hand, would require a bigger transistor and a larger area occupied on the chip by the front-end devices with a consequent limitation in the achievable integration density. As to the noise performances of the analog channels they feature an ENC of 350 electrons at zero detector capacitance and a dENC/dC12 sensitivity of about 30 eV/pF, measured with a nearly triangular weighting function of ≈ 10 μs baseline. The noise analysis of the analog channels leads to the conclusion that the dominant ENC contribution is brought about by the series 1/f-noise in the input N-channel MOSFET [3].

Although the noise performances of the chip are acceptable, a reduction in the dENC/dC12 sensitivity is, however, desirable in order to enable the chip to cope with larger detector capacitance without a sizable increase in equivalent noise charge. The series 1/f-noise could be substantially reduced at the expenses of a degradation in transition frequency and white noise contribution by using a P-channel MOSFET as the input device [4]. The advantage of depletion over enhancement MOSFETs as far as low frequency noise is concerned is still under investigation. These considerations have stimulated a growing interest for a low-noise development of the front-end chip based upon the idea of employing JFETs rather than MOSFETs for the input active element and for all other devices in the preamplifier that affect ENC to a significant extent.

The use of JFETs as input devices has several advantages over the MOSFET solution. First, JFETs have much less 1/f-noise than N-channel enhancement MOSFETs and are also better than P-channel MOSFETs. Secondly, the dominant ENC contribution in a JFET comes from the series white noise and can be effectively dealt with by the shaper with a triangular weighting function. Shaping, instead, is of little use with 1/f-noise. Thirdly, the thermal noise in a JFET is comparatively unaffected by the ionizing radiation to which the device is exposed. The 1/f-noise in an N-MOS, on the contrary, rapidly deteriorates under irradiation and this may force the replacement of the front-end chip in a situation, like that of LEP, where synchrotron radiation is present [5,6].

The design of the JFET-CMOS front-end chip is being presently carried on on the base of a process which makes P-channel JFETs available on the same chip with P and N channel MOSFETs. The resulting technology is very versatile, for it meets severe noise requirements with the JFETs, while it lends itself to the realization of the shaping and memory functions with the CMOS devices [7].
2. Characteristics of the JFETs compatible with the CMOS process

The design of JFET-CMOS front-end chip is being carried out as a cooperation with the Fraunhofer Gesellschaft, which matured a process that allows the realization of junction field-effect transistors and P and N-channel MOSFETs on the same chip. The JFETs belonging to this process will be referred to as CMOS-compatible JFETs. The actual monolithic process employs a P-doped substrate and N-type diffused wells house the P-channel MOSFETs, while the N-channel MOSFETs are realized in the substrate. The P-channel JFETs are obtained by implanting the channel in the N-well; their top gate is made by arsenic implant, and the well acts as a back-gate. The P-channel JFET, being inside the well, is naturally isolated from the other devices on the substrate. Very recently, also the N-chann

![Graphs showing characteristics of N-type and P-type JFETs](image)

**Fig. 2.** Drain static characteristics $I_D = I_D(V_{DS})$ and dependence of the gate current $I_G$ on $V_{DS}$ at constant gate-to-source voltage $V_{GS}$ for N-channel JFET (a), P-channel JFET (b).

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Fig. 3. Transconductance $g_m$ as a function of drain current. (a) N-channel JFET with gate length $l = 5 \mu m$ and gate width $W = 200 \mu m$. (b) P-channel JFET with $l = 4 \mu m$, $W = 200 \mu m$. (c) P-channel JFET with $l = 4 \mu m$, $W = 800 \mu m$. 
shown in fig. 2 for an N-channel and a P-channel JFET of equal gate widths, \( W = 200 \, \mu m \).

According to fig. 2, both devices have a pinch-off voltage of about 1.2 V and gate leakage currents well below 10 pA at a drain-source voltage lower than 3 V. The dependence of the transconductance \( g_m \) on the drain current \( I_D \) in the \( I_D \) range of interest for applications in high-density monolithic front-end chips, that is, \( I_D < 1 \, mA \) is plotted in fig. 3 for three different JFETs.

The curves of fig. 3 point out that large transconductance values are obtained at comparatively low drain currents. For instance, the JFETs of fig. 3 have transconductances of respectively 650, 480, 850 \( \mu A/V \) at \( I_D \) values of 100 \( \mu A \).

These large \( g_m / I_D \) ratios are an important feature in devices intended for low-noise monolithic circuits, as they guarantee a low white noise floor with a small power dissipation.

The advantage in using JFETs rather than MOSFETs from the \( 1/f \)-noise stand point is made clear by figs. 4 and 5. Fig. 4 compares the intrinsic \( 1/f \)-noise index \( H_f \) for four types of devices, P and N-channel MOSFETs, P and N-channel JFETs. \( H_f \) obtained as the product of the device input capacitance \( C_{i} \) and the coefficient \( A_f \) defining the spectral power density \( A_f / f \) of \( 1/f \)-noise, is an intrinsic feature of the type of device under consideration and is independent of its gate width \( W \).

Fig. 4 shows that, for each type of device, \( H_f \) is practically constant as the gate area is changed. All the devices of a given type have nearly the same gate length, 5 \( \mu m \) for the MOSFETs, 4 \( \mu m \) for the P-channel JFETs.

For the newly appeared N-channel JFET, only one value of \( W \) is available, \( W = 200 \, \mu m \). According to fig. 4, the \( H_f \) values for the N-channel enhancement MOSFET are well above those of the other devices and the JFETs are better than the P-channel MOSFET. The relative merit of JFETs over the MOSFETs is also evident from fig. 5 which compares the spectral power densities of four devices, two enhancement MOSFETs, P and N-channel and two JFETs, P and N-channel, all of equal area, \( W = 200 \, \mu m \), \( L = 4 \, \mu m \).

Further characterization of the noise behaviour of the CMOS-compatible JFETs was done through ENC measurements. The devices under test were employed as input elements of a purposely designed discrete charge-sensitive preamplifier where the noise contributions coming from the devices following the input one were made as small as possible. The preamplifier was associated with a semi-Gaussian amplifier whose shaping time constant \( \tau \) can be varied from 0.1 to 10 \( \mu s \). Some significant results are shown in figs. 6a to 6c. It is worth pointing out that, at a time constant of 1 \( \mu s \), the P-channel JFET with \( W = 200 \, \mu m \), \( L = 4 \, \mu m \) operated at \( I_D = 120 \, \mu A \) yields a dENC/d(\( C_{11} \)) sensitivity of \( \approx 25 \, e^/-pF \), which drops to less than \( 15 \, e^/-pF \) at \( \tau = 10 \, \mu s \).

The P-channel JFET with \( W = 1000 \, \mu m \) provides an ENC of only 600 electrons at \( \tau = 10 \, \mu s \) and \( C_{11} = 67 \, pF \) with a standing drain current of 90 \( \mu A \).

It can therefore be concluded that CMOS-compatible JFETs constitute a solution worth pursuing in the design of monolithic front-end chips for multi-detector systems with \( C_{11} \) values in the 10-100 pF range.

3. The JFET-CMOS preamplifier

The circuit diagram of the JFET-CMOS monolithic preamplifier is shown in fig. 7. The preamplifier consists of a charge-sensitive loop employing the P-channel JFET JF1, JF2, JF3 and the MOSFETs M1, M2, followed by an off-the-loop output buffer (JF4, JF5). The input JFET, JF1, the current source JF2 and the common-gate N-channel MOSFET M2 implement a
The complementary MOSFET switch M1, M2 serves the purpose of resetting the charge on the feedback capacitance $C_f$. During the reset phase, the preamplifier loop is in the condition of largest gain, and to prevent oscillation, an additional compensating capacitor $C_t$ is required. $C_t$ is connected between the high impedance point at the M1, M2 drains and ground through the M13, M14 switch when the reset is activated. Outside the reset phase the M13, M14 switch is open and $C_t$ accordingly disconnected. The JFETs JF1 and JF4 are a matched pair operating at the same standing current, which guarantees that the output dc voltage is close to zero with a high degree of accuracy and thermal stability. It is worth pointing out that this method of compensating the gate-to-source offset voltage in JF1 does not bring about a noticeable increase in noise as a balanced configuration at the preamplifier input would, instead, do.

In the present version, JF1 and JF4 have a gate width $W = 200 \, \mu m$ and a length $L = 4 \, \mu m$ and work at a standing current of about 100 $\mu A$. The drain current in JF1 is determined by the difference between the reference currents generated by JF2 (150 $\mu A$) and JF3 (80 $\mu A$). The standing current in JF4 is fixed by the current source JFS.

It has to be noticed that, beside the input element JF1, JF2 and JF3 affect the preamplifier ENC to a non-negligible extent and for this reason they are all JFETs. The noise sources in the common-gate amplifiers M1 and M2 have a less important impact on the

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**Fig. 6:** Equivalent noise charge as a function of the shaping time constant of a gaussian amplifier for P and N-channel JFETs at $C_f = 45$ pF and N-channel JFETs at $C_f = 45$ pF for four P-channel JFETs of different gate areas at $C_f = 45$ pF.

**Fig. 7:** JFET-CMOS monolithic preamplifier.
preamplifier ENC, so a MOSFET realization can be tolerated.

The preamplifier shown in fig. 7 occupies a silicon area of 0.18 mm² and dissipates a power of 2.8 mW. It features a dc forward gain of 85 dB and a risetime of 250 ns at a detector capacitance of 10 pF.

To evaluate the noise performances of the JFET-CMOS preamplifier and its relative merit compared to the CMOS version, the spectral power density of series noise referred to the input of both circuits has been measured.

As a comment to fig. 8, the JFET-CMOS preamplifier, in spite of a four time smaller area in the input device, 800 µm² against 3500 µm² has a considerably lower 1/f noise. The ENC performances of the JFET-CMOS preamplifier at C\textsubscript{11} values in the range of interest for microstrip applications are shown in fig. 9.

The ENC measurements were carried out with the preamplifier followed by a Gaussian shaper of time constant τ variable between 0.1 and 10 µs. According to fig. 9, the JFET-CMOS preamplifier at 5 µs time constant, which is in the region of processing times of interest for JFET, has about 500 rms electrons ENC at C\textsubscript{11} = 6 pF and dENC/dC\textsubscript{11} sensitivity of ~12 eV/pF.

To determine whether or not a sizable ENC contribution comes from elements other than JF1, the results of ENC tests averaged on several preamplifier samples and on several individual parts identical to JF1 have been compared. For these tests the individual parts were employed as input devices in a purposely designed charge-sensitive preamplifier with a negligible noise contribution from the following elements. A typical average behaviour for the individual parts and for the monolithic preamplifier is shown in fig. 10.

The curves of fig. 10 declare a non-negligible ENC contribution in the preamplifier due to the components that follow JF1. Among the measures that are being taken now to reduce such a contribution, an increase of a factor of 2 in the gate area of JF1, leaving the current levels unchanged, has been decided. This will result in a 50% increase of the JF1 transconductance with the consequence of a reduced relative importance of the noise generated in the components that follow.

An additional benefit related to this increase in the gate area is a reduction in the capacitive mismatch in the application with microstrip detectors (C\textsubscript{11} = 10 pF).

Moreover, according to the computer simulation, the augmented g\textsubscript{m} and the increase in τ\textsubscript{c} of JF1 related to the reduced current density will raise the dc forward gain to 95 dB.

4. Signal shaping following the preamplifier

During the development of the CMOS version of Aleph chip, the possibility of replacing the preamplifiers with the JFET-CMOS circuits was already being taken

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into account. Such a replacement was expected to change the relative importance of the ENC contributions brought about by white and 1/f-noise, from the case of 1/f-noise dominating in the CMOS preamplifiers to that of white noise dominating in the JFET-CMOS preamplifiers. While in the former situation the shaping cannot be expected to be of great help in improving the signal-to-noise ratio, it becomes of fundamental importance in the latter one. It was decided accordingly, to develop a shaper and to tailor it to the situation of a charge measurement in the presence of white noise [8].

The best estimator of the amplitude of the step developed by the detector current pulse across the integrating capacitor \( C_i \) in the presence of white noise averages the baseline at the preamplifier output prior to the event and after it and makes the difference of the two values. The resulting weighting function has a triangular or trapezoidal shape. The peculiar nature of the collider experiment, where the bunch crossings occur at predictable instants, makes the timing control of the averaging operations quite straightforward. The type of technology employed in both chips, lending itself to the realization of switched capacitor filters based upon CMOS devices suggests the idea of averaging the baseline through a sampled-data integration. To avoid the noise aliasing problems related with the discrete-time operation of the shaper, a bandwidth limitation has to be provided before it. This can be done in the simplest way by artificially increasing the frequency-compensation capacitor inside the charge-sensitive loop of the preamplifier.

In the existing CMOS version of the Aleph chip the shaper is implemented in the way shown in fig. 11a. It requires as many branches consisting of the series connection of a capacitor and a switch as the number of samples to be taken, four in the actual configuration. The branches are connected between the preamplifier output and the virtual ground-input of a gated integrator. The capacitors \( C_1 \) through \( C_4 \) have all the same value \( C \).

In the circuit of fig. 11a each branch performs a double sampling of \( V_{o1} \) one prior to the bunch crossing and one after it. The \( n \)th branch, after the twofold operation of the relevant switch, contributes to the voltage at the output of the integrator \( A_i \) with the term:

\[
-\frac{C}{C_o} \left[ V_{o1}(t') - V_{o1}(t) \right]
\]

The voltage \( V_i \) after the completion of the sampling cycle is:

\[
V_i(t_{SP}) = -\frac{C}{C_o} \sum_{i=1}^{n} \left[ V_{o1}(t') - V_{o1}(t) \right]
\]

and it turns out to be equal, in the case of an ideally noiseless preamplifier, to \((-C/C_i)Q/C_i\) \( Q \) being the charge delivered by the detector at \( t = t_{SP} \).

Fig. 11. Switched capacitor shapers. (a) Multicapacitor version. (b) Version employing a switched-mode integrator.

The shaper of fig. 11a can be employed in collider experiments that have a deterministic spacing between bunch crossing as well as in fixed target experiments with randomly distributed time intervals between the events. As a limitation, it requires one sampling branch for each sample. The shaper shown in fig. 11b, instead, is purposely intended for collider experiments and lends itself to the accurate realization of triangular weighting functions with large numbers of samples. Its operation can be described in the following way. Prior to the bunch crossing the switches \( S_1 \) and \( S_2 \) are controlled by the same clock phase. During each period of logic level HIGH in \( V_{L1} \) and \( V_{L2} \), with \( S_1 \) and \( S_2 \) simultaneously closed and \( S_3 \), \( S_4 \) open, a sample of \( V_{o1} \) is stored on the integrating capacitor \( C_2 \), changed in sign and multiplied by \( C_2/C_1 \).
After the occurrence of the bunch crossing, the phase of \( V_{1j} \) is reversed, which switches the integrator mode from the inverting to the non-inverting one. The samples taken from \( V_{1j} \) and multiplied by \( C_1/C_2 \) are now added to the voltage previously stored on \( C_2 \). At the end of the complete sampling cycle the voltage \( V_1 \) turns out to be:

\[
V_1(t_0) = \frac{C_1}{C_2} \sum_{j=1}^{n} V(t_j) - \sum_{j=1}^{n} V(t_j - t_0).
\]

In the ideal case of a noiseless preamplifier, \( V_1(t_0) \) would be equal to \( (C_1/C_2) \left( \frac{nQ}{C_1} \right) \), where \( Q \) is the charge delivered by the detector at \( t = t_0 \).

The actual shaper has some additional features, not shown in fig. 11 for the sake of simplicity. They make the operation highly insensitive to variations in the offset voltages of \( A_1 \) and \( A_2 \) and accurate also in the case of a low gain in \( A_2 \).

The shaper version of fig. 11b has been realized as an entirely CMOS monolithic structure. The two blocks existing now, the JFET-CMOS preamplifier and the CMOS shaper constitute the basic part of the analog channel. An individual channel has been set up and exhaustively tested. For the purpose, the two sequences of fig. 11b have been generated to provide the control signals for the shaper. Five pulses at a 2 \( \mu \)s spacing have been provided in each group of clock signals in the \( V_{11}, V_{12} \) sequences. The detector event has been simulated by injecting a known amount of charge at the preamplifier input during the empty interval between the two groups of clock pulses, where the bunch crossing is expected to occur. The voltage signal, which appears as the output of the integrator \( A_2 \), is shown in fig. 12.

The output of \( A_2 \), taken at an instant \( t_0 \) following the completion of the sampling cycle, was stored in a multichannel pulse height analyzer and the equivalent noise charge ENC was measured from the resulting Gaussian distribution of pulse amplitudes.

The analog channel was proven to have a low \( \text{dENC}/\text{d}C_{1j} \) sensitivity, \( = 11 \text{ e}^+/\text{pF} \), which, considered the comparatively long width of the weighting function adopted, confirms the good 1/f-noise performances of the JFET-CMOS preamplifier. The value of ENC at \( C_{1j} = 0 \) (600 electrons) is still large and was recognized to be affected to a sizeable extent by the 1/f-noise in the input long-tailed pair of the CMOS \( A_1 \) integrator. The two transistors in this long-tailed pair are N-channel MOSFETs of small area (\( W = 100 \mu \text{m}, L = 3.5 \mu \text{m} \)). To remove this problem, \( A_1 \) is now redesigned with P-channel MOSFETs of larger area as input active elements.

5. Conclusion

A JFET-CMOS microstrip front-end is now being developed. The two basic blocks in the analog signal acquisition and processing channels, the JFET-CMOS preamplifier and the CMOS sampled data shaper, have been implemented in monolithic form and tested together. Utilization of JFETs for all the functions that affect the preamplifier ENC has significantly reduced the effect of 1/f-noise with respect to the solutions entirely based on MOSFETs.

Partial structures consisting of a few channels on the same chip are now being realized and will serve the purpose of testing proximity effects and crosstalk limitations. In the meantime the design of the final JFET-CMOS multichannel chip is being carried ahead. The chip is intended to replace the CMOS front-end in the Aleph experiment during the foreseen machine shutdown.

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References


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