A 320-MHz Four-Paths Bandpass Sigma-Delta Modulator

Alfonso Centuori(1), Umberto Gatti(2), Piero Malcovati(3) and Franco Maloberti(1, 3)

(1) Department of Electrical Engineering, University of Pavia, Via Ferrata 1, 27100 Pavia, Italy
Tel. +39 0382 505205, Fax. +39 0382 505677, E-Mail: piero@ele.unipv.it

(2) Siemens Information and Communication Networks S.p.A., 20092 Cinisello Balsamo, Milano, Italy
Tel. +39 02 27337415, Fax. +39 02 27337151, E-Mail: umberto.gatti@icn.siemens.it

(3) Department of Electrical Engineering, PO Box 830688, EC33, Richardson, TX 75083-0688, USA
Tel. +1 972 883 2996, Fax. +1 972 883 2710, E-Mail: franco.maloberti@utdallas.edu

Abstract—In this paper we present a sigma-delta modulator for wide-band base transceiver station receivers. The modulator, based on a four-path architecture, achieves an equivalent sampling frequency of 320 MHz, although the building blocks operate at only 80 MHz. The circuit achieves 87 dB of signal-to-noise ratio with a signal bandwidth of 5 MHz centered around an intermediate frequency of 80 MHz. Behavioral simulations of the complete sigma-delta modulator, including the most important non-idealities of the building blocks are reported.

I. INTRODUCTION

Wide-band base transceiver station (BTS) receivers based on the software radio (SWR) technique [1] require an A/D converter with challenging specifications, particularly in terms of signal-to-noise ratio (SNR), sampling jitter, spurious-free dynamic range (SFDR) and intermediate frequency (IF) value (center frequency of the down-converted signal), which together with the SNR determines the maximum clock frequency. Obviously, practical limits in the implementation of the A/D converter impose a compromise between the above features. For a third-generation standard, such as the CWTS (China Wireless Telecommunication Standard) [2], reasonable specifications for the A/D converter in the BTS [3] lead to a signal bandwidth of 5 MHz, where three 1.28 Mb/s UMTS channels (1.6 MHz of bandwidth each) can be accommodated at the same time, a SNR better than 85 dB (equivalent to 14 bit), a sampling jitter around 0.5 ps and a SFDR better than 90 dBc. The positioning of the IF value is particularly important, since it has an impact on the RF filtering and the harmonic distortion. The choice of a proper IF value, indeed, leads to significant advantages. The following considerations were done in order to optimize the performances of the system:

• the anti-aliasing filter at the A/D converter input can be easily implemented using the SAW technology, but in this case the value of the IF value have to be high enough (practically, more than 60 MHz);

• the spectral interval between the useful RF band and the image band must be high enough to allow a sufficient image rejection, also leading to a high enough IF value;

• for achieving optimal A/D converter specifications, especially in terms of jitter, we would prefer a low IF value. Consequently, a practical choice of the IF value is around 80 MHz, as shown in Fig. 1. When using state-of-the-art commercially available A/D converters (with a maximum sampling frequency of 40 MHz), therefore, we are forced to consider for the conversion the third Nyquist zone.

However, although commercial A/D converters with the required specifications nominally exist, their linearity performances significantly degrade for such high IF. Moreover, using converters with a “lowpass” transfer function extended over the third Nyquist zone for handling signals with a bandwidth of 5 MHz is definitely a waste of resources. Therefore, it could be interesting to implement an A/D converter with a “bandpass” transfer function, such as a bandpass sigma-delta (ΣΔ) modulator, centred at the desired IF. Such a solution allows us to convert into the digital domain only the band around the IF, thus reducing the in-band thermal noise requirements (the thermal noise contributions outside the signal band are eliminated in the digital domain) and to optimize the quantization noise only in the band of interest.

In a ΣΔ modulator the clock frequency is essentially determined by the oversampling ratio (OSR) required to obtain the
desired SNR with a given signal bandwidth. A rough evaluation on a 4th-order bandpass \( \Sigma \Delta \) modulator architecture indicates that to achieve the desired SNR an OSR equal to 32 is needed. By considering a center frequency equal to a quarter of the clock frequency, the expected noise transfer function (NTF) of an \( n \)-th order bandpass modulator is of the type \((1 + z^{-2})^n\) with the zeros located at \( \pm j\). Multi-feedback, single-path implementations of a bandpass \( \Sigma \Delta \) modulator, such as the CRFB (cascade of resonators in feedback), the CRFF (cascade of resonators in feedforward) or the CI (cascade of integrators) [4, 5, 6], in this case lead to a prohibitive clock frequency with present technologies \((f_c = 320\, \text{MHz})\). We have therefore to consider sigma-delta modulators based on multiple paths. In particular, in this paper we propose a 4-path bandpass \( \Sigma \Delta \) modulator, where each path features a lowpass signal transfer function (and a highpass NTF) at a clock frequency \( f_c = 80\, \text{MHz} \). In this case, the overall equivalent sampling frequency is still 320 MHz, but all of the blocks operate at only 80 MHz, thus making this solution feasible with present technologies. The structure has been simulated in a MATLAB/SIMULINK environment and, also taking into account the non-idealities of the building blocks and the mismatches between the components, it satisfies the CWTS specifications.

II. FOUR-PATH ARCHITECTURE

The basic principle of the proposed sigma-delta modulator is shown in Fig. 2a, where four equal paths are connected in parallel as in interleaved A/D converters.

If \( T_s = 1/f_s \) is the sampling period at the modulator output, phases \( \phi_1 \) to \( \phi_4 \) have a period equal to \( 4\, T_s \) and are shifted each other by a quarter of the period. From the theory of multiple path circuits in the \( z \)-domain [7] it can be demonstrated that

\[
H_{TOP}(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = H_p(z^4)
\]

where \( H_p(z) \) is the transfer functions of the single path. If \( H_p(z) \) has lowpass shape, its attenuation spectra is replicated every \( f_s/8 \), as shown in Fig. 2b, thus leading to the desired bandpass NTF.

The main advantage of this solution is that every path operates at a frequency which is a quarter of the equivalent modulator frequency (in our case 80 MHz and 320 MHz, respectively). Moreover, the lowpass transfer function is inherently less sensitive to capacitance mismatches than the bandpass transfer function. Finally, as it will be shown later, this solution allows us to achieve the same SNR performance than single-path topologies with an higher order, with benefits in the stability and in the complexity of the design.

III. MODULATOR DESIGN

The design of the modulator in the first place requires the implementation of a NTF which fulfils the specifications for the single path. The STF is then automatically derived. From the converter SNR specifications we derived a highpass filter mask having a stop-band limit of 2.5 MHz, an in-band attenuation of 85 dB, a ripple of 0.5 dB and a pass-band limit at 12 MHz \((f_s = 80\, \text{MHz})\). In the frequency domain the couples of zeros are located at 1.1 MHz and 2.5 MHz. After obtaining the position of poles and zeroes, we have to define a suitable topology to implement the NTF which guarantees a sufficient freedom in determining the coefficients. By using conventional CRFB, CRFF or CI architectures, we obtain an equations system which cannot be solved, thus making impossible the synthesis of the calculated polynomials. Thus, a new topology has been defined, where the feedback paths contain not only a gain factor, but also more complex transfer functions \( H_1(z) \) and \( H_2(z) \). The block diagram of the proposed structure is shown in Fig. 3, while Fig. 4 illustrates the schematic diagrams of blocks \( H_1(z), H_2(z), H_3(z) \) and \( H_4(z) \).

Finally, we used an 8-levels quantizer block to achieve the desired SNR and to ensure the stability of the modulator. This choice also avoids the presence of tones, since it reduces the power of the quantization noise. The value of the modulator coefficients are reported in Fig. 3.

IV. SIMULATION RESULTS

The proposed bandpass \( \Sigma \Delta \) modulator has been extensively simulated using a toolbox, developed in the MATLAB/SIMULINK environment, devoted to the fast analysis of SC \( \Sigma \Delta \) modulators [8]. The general topology used in the simulations
The basic blocks used for the simulation take into account a number of non-idealities, namely $kT/C$ noise, clock jitter, operational amplifier non-idealities (noise, finite gain, finite bandwidth, finite slewing rate and saturation) and DAC errors. The modulator output spectrum in the ideal case with a sinusoidal input signal at 80.17 MHz is shown in Fig. 6a, where is applied. The achieved SNR is higher than 105 dB, which is equivalent to 17 bits of resolution. The correct location of the zeros is evident in Fig. 6b. Moreover, it can be observed that no spur tones are present in the spectrum.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling capacitor for $kT/C$ noise</td>
<td>1 pF (65 μV/√Hz)</td>
</tr>
<tr>
<td>Operational amplifier gain</td>
<td>80 dB</td>
</tr>
<tr>
<td>Operational amplifier bandwidth</td>
<td>600 MHz</td>
</tr>
<tr>
<td>Operational amplifier slewing rate</td>
<td>400 V/μs</td>
</tr>
<tr>
<td>Clock jitter</td>
<td>0.1 ps</td>
</tr>
<tr>
<td>DAC error</td>
<td>±0.05%</td>
</tr>
</tbody>
</table>

| Tab. 1 - Non-idealities used for the simulation of the 4-paths modulator |

To validate the proposed idea in real conditions, we introduced the non-idealities reported in Tab. 1. Moreover, a coefficient mismatch of ±1% among the four branches has been considered in the simulations. The output spectrum of the modulator obtained under these operating conditions is shown in Fig. 7. The modulator achieves again a SNR better than 87 dB and an equivalent resolution of 14 bits.

**V. CONCLUSIONS**

In this paper we presented a four-path sigma-delta modulator for wide-band base transceiver station receivers based on the software radio architecture. The modulator features 5 MHz of bandwidth centered around an intermediate frequency of 80 MHz and achieves 87 dB of signal-to-noise ratio. The performances of the sigma-delta modulator have been verified.
with behavioral simulations of the complete circuit, including the most important non-idealities of the building blocks.

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REFERENCES
