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A 1.8V, 1MS/s, 85dB SNR 2+2 Mash ΣΔ Modulator with ±0.9V Reference Voltage

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Abstract

A 1.8V, 1MS/s, 85dB SNR 2+2 mash ΣΔ modulator with ±0.9V reference voltage is realized by using the swing reduction structure. This structure limits the output swing of all the integrators within half the reference voltage. Thus, low voltage and high speed operation is possible with even high reference voltage without degrading the performance of the modulator. The circuit is fabricated in CMOS 0.35um process with chip size of 2.5×2.5mm².

Keywords: ΣΔ modulator, swing reduction structure, reference voltage, low voltage, high speed and SNR.

Introduction

An essential design goal in low voltage and high speed ΣΔ modulators is maximizing the reference voltage while minimizing the output swing of the integrators: the dynamic range of the modulator increases with even low supply voltages. For conventional single-bit high-order modulators, the output swing of the integrators is usually larger than 1.6 times the reference voltage [1]. Large integrator output swing exceeding the supply limit causes harmonic distortion: when the output of the integrator saturates the input charge is not completely transferred. In addition, assuming the maximum integrator output swing is around 0.8VDD, where VDD is the supply voltage, the maximum usable reference is only ±0.25VDD. Also, the op-amps must provide high GBW and slew rate, since improper settling and slewing of the integrator output cause performance degradation. Multi-bit modulators can reduce the output swing of the integrators thus relaxing the dynamic range and slewing requirements, but multi-bit solutions force the use of dynamic element matching and digital error correction schemes, which increases the complexity of the design [2],[3].

In this paper, a 2+2 mash ΣΔ modulator using a swing reduction method is proposed, which can limit the output swing of all the integrators within half the reference voltage. Therefore our design is able to use a reference voltage (±0.9V) as large as the supply voltage (1.8V). Moreover, the swing reduction significantly alleviates the GBW and slew rate requirements of the op-amps.

Integrator Swing Reduction Structure

Fig. 1 shows a general second order ΣΔ modulator and its modification for achieving the swing reduction [4]. The signal from the feedback loop is not added to the first integrator input, but it is processed in the digital domain with the same transfer function of the first integrator and added to the input of the second integrator after passing through a DAC. Freeing the first integrator by the global feedback enables an effective local control of the first integrator output voltage. Here, different local feedback values +VREF, -VREF, or 0 are generated depending on the sign of the input and the first integrator output. If the input and the first integrator output are both positive or negative compared to the mid-supply voltage, -VREF or +VREF is fed back to the first integrator input. This kind of control is very effective. It limits the output swing of the first integrator within half the reference voltage regardless of the input value, if the input level is within ±VREF which is the general case for ΣΔ modulators. On the other hand, if the sign of the input and first integrator output is different, the feedback is 0, since for this case the output of the first integrator will not exceed half the reference voltage even without the aid of the local feedback.

The effect of the local control is compensated with the digital processing section. The local feedback signal is processed with the global feedback signal, which is the bit-stream output of the modulator, to cancel the local feedback effect. The processed signal is injected at the input of the second integrator through a low resolution DAC. Seven output levels ±1.5VREF, ±VREF, ±0.5VREF, and 0 are sufficient for the DAC. As a result, the DAC output cancels the local feedback effect and restores the global feedback at the input of the second integrator. Therefore, the output swing of the first integrator is limited within half the reference voltage, while maintaining the same bit-stream output as the conventional second order counterpart.
Modulator Design

A. Proposed Architecture

The swing reduction technique has been applied to a 2+2 mash ΣΔ modulator. Fig. 2 shows the block diagram of the circuit. The modulator uses the integrator swing reduction in each stage of the mash arrangement. Therefore, the output swing of the first and third integrator is limited to half the full reference voltage. In addition, the output swing of the second and fourth integrator is reduced within half the reference voltage by optimizing the integrator gain coefficient to 0.25 and 0.125, respectively. Moreover, the inter-stage gain factor and the second stage gain factor are increased to 2 and 4, respectively to maximize the SNR of the modulator by compensating the low integrator gain coefficient of the second and the fourth integrator [5].

Fig. 3 shows the simulated output density of the first and third integrator for the proposed 2+2 mash ΣΔ modulator and the conventional 2+2 mash ΣΔ counterpart. The results refer to a sinusoidal input, which is 6dB below the full scale. As shown from the results, the proposed modulator the output swing of the first and third integrator does not exceed ±0.5VREF, while for the conventional modulator it is around ±1.35VREF and ±1.75VREF, respectively.

The saturation of the op-amps input-output response due to supply voltage reduction degrades the SNR of the modulator. This effect is studied using the behavioral level ΣΔ modulator model with a hard clipping above a given level. Fig. 4 compares the SNR degradation for the proposed 2+2 mash ΣΔ modulator and the conventional counterpart. Both cases the reference voltage is set to ±0.9V with the clipping level decreasing from 4V to 0.5 V. The result shows that the clipping voltage should be at least 3.5V for the conventional modulator to operate properly, while the proposed modulator does not show significant degradation even with a supply voltage of 1.5V.

A mismatch between the first analog integrator and its digital equivalent also causes a SNR worsening. Namely a gain error is the most critical limitation. A mismatch in the third integrator is less important since it processes a quantization noise which has already passed through a noise shaping function. Fig. 5 shows the simulation results for mismatches up to 1%. The mismatch that causes 1 bit loss in the resolution of the modulator is 0.15%, which is expected for the real circuit.

![Fig. 2 Block diagram of the proposed ΣΔ modulator.](image)

![Fig. 3 Number of occurrence vs. output level of integrator 1&3.](image)

![Fig. 4 SNR degradation vs. supply voltage.](image)

![Fig. 5 SNR & SFDR vs. gain mismatch between the first analog integrator and the digital integrator.](image)
B. Low Voltage SC Integrator and Op-amp

The low voltage SC integrator is realized by using boosted clocks for the CMOS transistor switches in the signal path and employing op-amps with different common mode input and output voltages [6]. The input common mode voltage of the op-amp is lowered to 0.3V, which is well below the mid-supply voltage (0.9V), in order to ensure proper charge transfer for the virtual ground connected NMOS transistor switches. In addition, to leave maximum headroom for both sides of the integrator swing, the output common mode voltage of the op-amp is set to the mid-supply level. The size of the sampling capacitor for the first integrator is set to 0.8pF, considering the kT/C noise and the settling time of the integrator.

The op-amp used for the SC integrator is a 2-stage fully-differential configuration, with a folded cascode amplifier in the first stage and a common source amplifier in the second stage. The common mode feedback is implemented by a switched capacitor scheme for each stage [7]. Also, a PMOS transistor is used for the input stage for favoring a low input common mode voltage and for reducing the 1/f noise. The performance of the op-amp shows a DC gain of 72dB, 350MHz GBW with 2pF load and 58° phase margin.

C. Local Feedback and Digital Integrator

Fig. 6 shows the block diagram of the digital section. It includes the local feedback and digital integrator. An identical digital section is used in each stage, which generates the control clocks for the feedback switches included in the first and third integrator and the DAC switches for the second and fourth integrator. While the analog integrators repeat the sampling and integration based on the 2-phase non-overlapping clocks, φ1 and φ3, the local feedback generates the output at the falling edge of φ3, referring to the modulator input and the integrator output. The digital integrator operates at the rising edge of φ3, and the control clocks for the DAC are generated at the falling edge of φ3. Here, the integrator coefficient equal to 0.5 is realized in the digital domain by doubling the bit-stream output at the output node of the digital integrator.

To enable the operation of the comparator after the integrator outputs are completely settled to their final value, a delayed version of φ2 is used for the comparator enable clock. With this scheme, the digital section is exactly synchronized with the analog section.

Experimental Results

Fig.7 shows the chip micrograph of the circuit. It is fabricated in 0.35µm CMOS technology - 2 poly, 4 metal process. The chip size is 2.5 x 2.5mm² with a core size of 1.8 x 1.7mm². The overhead due to the additional integrator output swing reduction circuitry is only about 20% of the total core area. The power consumption of the chip is 120mW for the analog section and 30mW for the digital section with a sampling clock of 64MHz. The power level can be reduced with a power aware design, but the aim of this work is to demonstrate the swing reduction method.

Fig. 8 shows the measured output waveform of the first and third integrator with reference voltage of ±0.9V. The amplitude of the input sinusoidal signal is 0.9Vp with common mode level of 0.9V. Measures confirm that the output swing of the first and third integrator is limited within half the reference voltage, which is ±0.45V.

Fig. 9 is the output spectrum of the modulator for -6dB, 238.281kHz input. The peak SNR is 85.7dB for OSR = 64 and decreases to 72.4dB for OSR = 32. Moreover a third harmonic term, which is about 82dB below the input signal level is observed. The drawback is explained by a 0.25% mismatch between the gain of the analog integrator and the digital counterpart in the swing reduction circuit. An improved layout technique based on the use of smaller and inter-digitized unit capacitors would reduce the mismatch to 0.1% thus improving the peak SNR to 91dB and reducing the third harmonic tone to 96dB below the input level - Fig. 5.

Fig.10 shows the SNR vs. input signal amplitude. The dynamic range is 87dB for OSR = 64 and 74dB for OSR = 32. TABLE I shows the performance summary of the proposed 2÷2 mash ΣΔ modulator.
TABLE I
PROPOSED ΣΔ MODULATOR PERFORMANCE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak SNR</td>
<td>85.7dB</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>87.0dB</td>
</tr>
<tr>
<td>OSR</td>
<td>64</td>
</tr>
<tr>
<td>Sampling Frequency</td>
<td>64MHz</td>
</tr>
<tr>
<td>Signal Bandwidth</td>
<td>0.5MHz</td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>±0.9V</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>150mW</td>
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<tr>
<td>Chip Size</td>
<td>2.5 x 2.5mm²</td>
</tr>
<tr>
<td>Core Size</td>
<td>1.8 x 1.7mm²</td>
</tr>
<tr>
<td>Technology</td>
<td>CMOS 0.35μm</td>
</tr>
</tbody>
</table>

Conclusions

A single-bit 2+2 mash ΣΔ modulator, which can limit the output swing of all the integrators within half the reference voltage by using the integrator swing reduction structure along with proper integrator gain coefficient optimization, is proposed. It is shown that the modulator can operate with reference voltage equal to the supply voltage without distorting the output of the integrator. The peak SNR of the proposed modulator is 85.7dB with OSR = 64. The reduced output swing of the integrator is also beneficial for high speed operation, since the GBW and slew rate requirement of the op-amp are significantly alleviated.

References