A MIXED-MODE A/D CONVERTER WITH SELF-TESTING CAPABILITY

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Abstract

This paper describes a 15-bit resolution self-calibrated A/D conversion system which can also realise the complementary D/A conversion. This makes it possible to implement a closed loop D/A + A/D conversion which can be used for performing a self-testing of the converter.

1. INTRODUCTION

For high resolution A/D conversion, self-calibrating systems have great advantages since they can guarantee full resolution independent of temperature and ageing [1,2]. The architecture proposed in this paper is based on the successive approximation algorithm using an effective 15-bit Binary-Weighted Capacitor (BWC) array. For limiting the capacitance spread, the 15-bit BWC array is segmented into a Main-Array (MA) for the M Most Significant Bits (MSB’s) and a Sub-Array (SA) for the L=15-M Least Significant Bits (LSB’s). The length L=7 of the BWC SA is determined such that the worst-case matching accuracy of the capacitance ratios guarantees the required resolution and linearity specifications of the converter. Since in the M-bit (M=8) BWC MA it is not possible to guarantee the full resolution and linearity specifications of the converter an additional R-bit (R=9) Auxiliary-Array (AA) is utilised to provide a means for measuring, and then correcting, the errors that are associated with the capacitors of the MA. This architecture can also be reconfigured as a D/A converter to realise the complementary 15-bit D/A conversion. Therefore, by applying digital codes to the D/A converter, putting the resultant output analogue voltage back to the A/D converter and comparing the output code with the applied one, useful information for characterising the functional performance of the circuit can be extracted.
2. SELF-CALIBRATION PROCEDURE

Under the command of the microcontroller, the procedure for calibrating the M-bit MA can be divided into a phase for measuring the error voltages, a phase for digitizing such error voltages and, finally, the calibration phase. The measuring phase is carried-out sequentially from the MSB $a_M$ to the LSB $a_1$. The sequence of operations that allow the determination of the residual voltage in the array is schematically illustrated in Fig.1, for the case of the MSB. Such residual voltage $V_{xM}$ can be related to the voltage error $V_{eM}$ associated with capacitor $C_M$ [1,2]. Once this error voltage has been determined, capacitor $C_M$ remains connected to ground. Then, this procedure repeats sequentially for all the remaining capacitors in the MA, and always leaving the previously measured capacitors connected to ground. In order to obtain the digital representation of the error voltages, it is necessary to carry-out a phase of digitization. This is implemented by means of the R-bit AA using a successive approximation A/D conversion algorithm. The digital representations of the residual voltages, $DV_{xM}$, are then used to compute the corresponding digital error voltages, $DV_{eM}$, which are stored in the calibration memory (RAM) of the system. For a given configuration of the M-bit MA, either during an A/D conversion cycle or during D/A conversion, the total resulting error can be derived by summing the error voltages corresponding to the active bits of the input digital word. The calibration phase consists, therefore, of applying such error voltages to the AA in order to subtract from the current conversion result the error corresponding to the total capacitance error.

3. A/D CONVERSION

The A/D conversion can be divided into a phase for sampling the input signal voltage and a phase for converting such signal. Fig.2-a illustrates the sampling phase where the MA samples the input voltage while the sign capacitor $C_M$ samples the reference voltage $V_{ref}$. Both of the amplifiers are auto-zeroed in order to compensate for their offset voltage errors. Since the reference voltage is positive, and the SA is actually an inverting amplifier, the $b_j$ LSB's must be complemented and, during the sampling phase, the capacitors of the SA are all connected to the reference voltage. Similar considerations also apply to the AA, except for the case of the sign bit which is effectively required to produce a negative contribution.
After the sampling phase there is the conversion phase, during which the system is connected as shown in Fig.2-b. Since all the capacitors of the MA, excluding the sign capacitor, are switched to ground, a nominal voltage \( V_N = -(1/2) \cdot (V_{IN}) \) is produced at the input of the comparator. Then, the successive bits are tested according to the classical successive approximation algorithm. When each bit is being tested the digitized error voltage of the corresponding capacitor is fetched from memory, added to the accumulated error due to the capacitors that have already been tested, and then applied to the AA for producing the required calibrating voltage.

4. D/A CONVERSION AND SELF-TESTING

For D/A conversion the system is reconfiguration as illustrated in Fig.3. The resulting circuit consists of a two stage amplifier whose gain can be programmed through the BWC arrays. In the first phase, illustrated in Fig.3-a, both of the amplifiers in the circuit are auto-zeroed for compensating their offset voltage. During the next phase, illustrated in Fig.3-b, the sum of the error voltage corresponding to the active bits in the MA is applied to the AA, thus performing the calibration.

Fig.4 represents the block diagram of the system for self-testing. Firstly, for an input digital word generated by the Digital Patter Generator, the system, configured as a D/A converter, produces an intermediate voltage that is sampled by an auxiliary sample and hold circuit. This analogue voltage is subsequently converted into a digital word when the system is reconfigured as an A/D converter. The resulting output digital word is then compared with the originally generated digital word. To prevent that the errors on the A/D conversion cycle compensate those on the D/A conversion cycle, the D/A conversion is actually implemented as an inverting A/D conversion. The resulting offset voltage of all three operations, D/A conversion, sample and hold and A/D conversion, can be compensated by applying the code zero for D/A conversion and then find the appropriate code to apply to the auxiliary summing input in order to eliminate the output offset voltage. Under such condition, several functional tests can then be realized to produce useful information for characterising the operation of the A/D converter. For example, by applying a given sequence of codes an error associated with one bit can be detected and its value readily identified, even for errors as low as 1/4 LSB. During the fabrication phase the testing set-up can be provided by an external sample and hold circuit, a low resolution D/A converter and a microcontroller. However, there is also
the possibility of implementing a self test on-chip. In this case the auxiliary sample and hold and D/A converter circuits are included on chip and the control logic applies successively all the input codes. In this way, it is possible to detect an integral nonlinearity error on the A/D conversion larger than 1/2 LSB by simply checking if the output codes do not correspond to the codes applied at the input.

5. CONCLUSIONS

This paper describes a high resolution self-calibrating A/D conversion system which also allows the realisation of the complementary D/A conversion function. This can be used for testing purposes without the need of an auxiliary D/A converter with higher resolution thereby substantially reducing the cost of manufacture and testing. An on-chip self testing capability is also readily implemented using dedicated sample and hold and low resolution D/A conversion circuits.

References


![Diagram of testing configuration](image-url)
Fig. 2 A/D Conversion Operation

Fig. 3 Inverting D/A Conversion Operation

Fig. 5 Layout of the analogue part of the system including the capacitor arrays, high resolution comparator and associated switches