
©20xx IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.
USE OF DYNAMIC ELEMENT MATCHING IN A MULTI-PATH SIGMA-DELTA MODULATOR

Vincenzo Ferragina(1, 2), Andrea Fornasari(1), Umberto Gatti(4), Piero Malcovati(1) Franco Maloberti(1, 3) and Luigi Monfasani(1)

(1) Department of Electrical Engineering, University of Pavia, Via Ferrata 1, 27100 Pavia, Italy Tel. +39 0382 505205, Fax. +39 0382 505677, E-Mail: p.malcovati@ele.unipv.it, l.monfasani@ele.unipv.it, a.fornasari@ele.unipv.it
(2) Studio di Microelettronica, STMicroelectronics Via Ferrata 1, 27100, Pavia, Italy E-Mail: v.ferragina@ele.unipv.it
(3) Dep. of Electrical Engineering University of Texas at Dalls, PO Box 830688, EC33, Richardson, TX 75083-0688, USA Tel.+1 972 883 2996, Fax. +1 972 883 2710, E-Mail: franco.maloberti@utdallas.edu
(4) Siemens Mobile Communications S.p.A., 20092 Cinisello Balsamo, Milano Italy, Tel. +39 02 27337415, Fax +39 02 2739829, E-Mail umberto.gatti@siemens.com

ABSTRACT

This paper describes the use of dynamic element matching in a multi-bit, multi-path sigma-delta modulators. The technique achieves noise shaping and enables the use of elements with 0.5% mismatch. Simulation results at the behavioral and gate level shows the possibility to achieve an SNR as large as 85 dB and SFDR of 90 dB with a 320 MHz equivalent clock frequency.

1. INTRODUCTION

Future electronic instruments and telecommunication devices require integrated analog-to-digital converters (ADC) with high speed and, at the same time, high linearity and resolution. Using time-interleaved architectures is an effective way for increasing the conversion rate: many ADCs operate in parallel, using different clock phases [1], as show in Fig. 1.

The analog demultiplexer selects each ADC for a low speed operation. The digital multiplexer interleaves the digital output of the ADCs, thus producing the overall A/D conversion result. Any type of ADC can be used. Each of them operates at a to \( f_{	ext{ck}}/M \), where \( f_{	ext{ck}} \) is the overall sampling frequency and \( M \) is the number of channels (or paths) used.

It is well known that multiple-path circuits achieves, in the sampled-data domain, the \( z \rightarrow z^N \) transformation. Therefore, if \( H_p(z) \) is the transfer function of the single path, the total transfer function becomes

\[
H_{\text{TOT}} = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = H_p(z)^N, \quad (1)
\]

if \( H_p(z) \) is low-pass, the response folds at multiples of \( f_{	ext{ck}}/M \), thus leading to a band-pass transfer function centered around \( f_{	ext{ck}}/4 \) (the relative NTF is shown in Fig. 2a).

Using sigma-delta (\( \Sigma \Delta \)) modulators in the single path (Fig. 2b shows the architecture) leads to the following benefit [2]: multiplexing at the output the oversampled bit-streams leads to a band-pass total transfer function exactly as when using the Nyquist-rate decimated signals. Moreover, since the sensitive to component mismatch of the low-pass \( \Sigma \Delta \) modulators is pretty low, dynamic range and stability are an affordable issue.

Figure 1. Block diagram of multi-path ADC

![Figure 1. Block diagram of multi-path ADC](image)

Figure 2. Four-path \( \Sigma \Delta \) modulator (b) and its Noise Transfer Function (a)

![Figure 2. Four-path \( \Sigma \Delta \) modulator (b) and its Noise Transfer Function (a)](image)
For a third-generation mobile communication standard, such as the CWTS (China Wireless Telecommunication Standard), specifications for the A/D converter in the base transceiver station require using a signal bandwidth of 5 MHz, centered around 80 MHz, thus enabling the conversion of three 1.28 Mb/s UMTS channels (1.6 MHz of bandwidth each). Specs are not extremely demanding: the SNR must be 85 dB (equivalent to 14 bit), the sampling jitter around 0.5 ps, and a SFDR more than 90 dBc.

However, achieving these specifications, require suing in the multi-path architecture a multi-bit quantizer in the LP-ΣΔ, of n each path. Unfortunately, using multi-bit quantizer leads to a multi-bit DAC in the feedback path. Since a multi-bit DAC is not intrinsically linear trimming or dynamic element matching (DEM) should be used.

Tab. 1 summarizes the main features of a possible system capable to meet the above mentioned specifications. Observe that 4 path working at 80 MHz clock leads to an equivalent clock frequency of 320 MHz. Moreover, 14 bit demand for a fourth order modulator with a 9-level quantizer.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency</td>
<td>320 MHz</td>
</tr>
<tr>
<td>Center frequency</td>
<td>80 MHz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>5 MHz</td>
</tr>
<tr>
<td>Quantizer</td>
<td>9 levels</td>
</tr>
<tr>
<td>Order (of each path)</td>
<td>4</td>
</tr>
</tbody>
</table>

Table 1. Characteristic of a four-path band-pass ΣΔ modulator for UMTS base transceiver stations

The architecture of the single-path modulator was studied previously and discussed in [2]. This work present the use of a suitable DEM technique for meting the SFDR specifications.

2. DEM AND NOISE-SHAPING

Various papers show how to implement the DEM concept and how to obtain the same noise-shaping feature exploited in ΣΔ modulators for the errors due to DAC’s element mismatch [3, 4]. Reference [5] uses a suitable logic to control the DAC element selection. The technique, applied to unipolar signals, spreads the power of the mismatch error over the whole modulator bandwidth with a suitable shaping of the power spectral density.

Unfortunately the above mentioned method cannot be directly used for bipolar signals. Fig. 3 shows the block diagram of the differential DAC that is used in our system. The left plate of each capacitor is connected to \( t_i \) \( V_{ref} \), \( t_i \) represents the value of the \( i \)-th capacitor selection signal, its possible values are \{-1,0,+1\}, and \( V_{ref} \) is the voltage reference.) The selection vector satisfies the condition

\[
\sum_{i=1}^{N} t_i = N_s, \quad (2)
\]

Therefore, the voltage at the output of the DAC for a generic level \( k \) is

\[
V_{DAC}(k) = \sum_{i=1}^{N} t_i(k) \cdot \frac{C_i}{C_{tot}} \cdot V_{ref} \quad k = 1 \ldots s, \quad (3)
\]

\( s \) is the number of output levels of the DAC, \( C_i \) is the \( i \)-th capacitor and \( C_{tot} \) is the sum of all the capacitances, given by

\[
C_{tot} = \sum_{i=1}^{N} C_i. \quad (4)
\]

The mismatch between the capacitors, \( \varepsilon_i \), is defined by

\[
C_i = C_{tot}/N + \varepsilon_i, \quad (5)
\]

with the condition that

\[
\sum_{i=1}^{N} \varepsilon_i = 0. \quad (6)
\]

Combining Eqn. (3) and Eqn. (5) gives

\[
V_{DAC}(k) = \sum_{i=1}^{N} t_i(k) \cdot \frac{V_{ref}}{N} + \sum_{i=1}^{N} t_i(k) \cdot \varepsilon_i \cdot \frac{V_{ref}}{C_{TOT}/N}, \quad (7)
\]

with \( k = 1 \ldots s \).

The first term of Eqn. (7) is the correct output of the DAC; the second is the error caused by the mismatch between capacitors. Using dynamic element matching the system uses a suitable selection signal \( t_i \) that shapes the error power outside the band of interest.

3. DEM SELECTION ALGORITHM

Fig. 4 shows the block diagram of the DAC element selection described in [6]. This paper uses the same approach adapted to bipolar signals. In the diagram \( v \) is the \( N \)-bit digital word received from the ADC; \( t \) is the noise shaped control of the unity elements of the DAC.

The noise-shaping transfer function of the system is \( H \). The element selection logic itself is essentially a set of \( N \) digital ΣΔ modulators, each providing the noise-shaping transfer function \( H \).

The input of the vector quantizer is a set of \( N_s \) digital num-
bers, \( sy \), which value accomplishes the use of each unit element. The input word \( v \) establishes how many capacitors must be used in the digital-to-analog conversion. The combination of \( sy \) and \( v \) leads to the to elements selection by sorting the elements of the vector \( sy \) and enabling the ones with the largest score for usage.

The complexity of the hardware for the vector quantizer algorithm is proportional to \( N \log_2 N \).

By inspection of the block diagram we have

\[
se = t - sy .
\]

(8)

The element error is the difference between the actual element value and the average

\[
\varepsilon_i = C_i - \frac{C_{tot}}{N} .
\]

(9)

The vector \( de \) is the set of \( \varepsilon_i \). Moreover, the sum of the elements of \( de \) is zero

\[
[1 \ldots 1] \cdot de = 0 .
\]

(10)

The z-transform of the output of the element selection logic can be expressed by

\[
sy = su \cdot [1 \ldots 1] + (H - 1) \cdot se .
\]

(11)

Therefore, combining Eqn. (8) and Eqn. (11) we obtain

\[
t - se = su \cdot [1 \ldots 1] + (H - 1) \cdot se ,
\]

(12)

from which we can derive the value of the output of the system \( t \)

\[
t = su \cdot [1 \ldots 1] + H \cdot se .
\]

(13)

Its z-transform is

\[
T(z) = SU(z) \cdot [1 \ldots 1] + H(z) \cdot SE(z) .
\]

(14)

Therefore, the output of the DAC is the sum of the nominal term and the error term. Since

\[
DT(z) = T(z) \cdot ([1 \ldots 1] + de) .
\]

(15)

the constraint on the vector quantizer results in

\[
T(z) \cdot [1 \ldots 1] = N_y(z) ,
\]

(16)

Using Eqn. (10), Eqn. (14) and Eqn. (16), Eqn. (15) becomes

\[
DT(z) = N_y(z) + H(z) \cdot (SE(z) \cdot de) ,
\]

(17)

which shows that the DAC output is the input signal \( N_y \), (\( N_y, V_{ref} \) is the DAC output) plus the noise term shaped by \( H \).

The extension of the method to bipolar signals requires to change the sign not only in the \( v \) and \( t \) vectors but also in the score for use. As a result when the input is negative the elements used are the ones with lower score of use.

### 4. DEM IMPLEMENTATION

A behavioral simulation of the selection algorithm validated the approach. The LP-ΣΔ modulator has a 9-level DAC and a first-order mismatch noise-shaping. Fig. 5 shows the block diagram of the hardware. For a first order shaping the transfer function \( H - 1 \) is simply

\[
H - 1 = (1 - z^{-1}) - 1 = z^{-1}
\]

(18)

Fig. 6 shows that degradation of the single path caused by a 0.5% element mismatch (the SNR is reduced by 18.2 dB). The use of DEM makes the performance degradation negligible (Fig. 7.) The SNR achieved with DEM is around 89.0 dB (which means resolution of about 14.5 bits).
MHz is as low as 70.0 dB (Fig. 8), the SNR becomes next to 87.5 dB (corresponding to around 14.0 bits) when the DEM algorithm is used (Fig. 9).

The simulation results refer to a VHDL description of the selection algorithm and its synthesis. The post-synthesis results are shown in Fig. 10. The obtained SNR is around 88.5 dB corresponding to about 14.5 bits.

The silicon area for the complete DEM algorithm for a 9-level DAC is 210 $\mu$m x 210 $\mu$m when using a conventional 0.18 $\mu$m CMOS technology.

5. CONCLUSIONS

This paper shows the benefit of using dynamic element matching with bipolar input signals in multi-path $\Sigma\Delta$ modulators. Simulation results both at the behavioral and gate level confirmed the effectiveness of the method. The SNR and the SFDR does not degrade even with mismatched as large as 0.5%.

ACKNOWLEDGEMENTS

The research was partially supported by MEDEA+ in the frame of Project ANASTASIA+ A510.

REFERENCES


