M. Kinyua, F. Maloberti, W. Gosney: "**Digital background auto-calibration of DAC non-linearity in pipelined ADCs**"; Proc. of the 2004 International Symposium on Circuits and Systems, ISCAS 2004, Vol. 1, 23-26 May 2004, pp. 13-16.

©20xx IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

DIGITAL BACKGROUND AUTO-CALIBRATION OF DAC NON-LINEARITY IN PIPELINED ADCs

Martin Kinyua¹, Franco Maloberti² and William Gosney³

¹Texas Instruments Inc, Dallas, TX

kinyua@ti.com

²Department of Electrical Engineering, The University of Texas at Dallas
Richardson, TX

franco.maloberti@utdallas.edu

³ Department of Electrical Engineering, Southern Methodist University
Dallas, TX

wmg@seas.smu.edu

ABSTRACT

In this paper, a digital background auto-calibration method that computes mismatch between the elements of the inter-stage Multiplying-Digital-to-Analog Converter (MDAC) as commonly employed in pipelined Analog-to-Digital Converters (ADCs) and then applies a linearizing algorithm in the digital domain is described. The calibration does not interrupt the normal operation of the ADC and is performed periodically, thus inherently able to track changes in the operating conditions of the device, a major limitation of one-time calibration approaches. This scheme requires an extra MDAC element and a reference element. The MDAC mismatch is digitized by the succeeding stages of the pipeline and subsequently digitally extracted. The accuracy of the calibration algorithm depends on the number of clock periods used for each calibration session. Longer sessions lead to better accuracy with the trade-off being additional digital circuitry. System simulation results demonstrate validity of the approach.

1. INTRODUCTION

In this paper, a method to calibrate pipelined ADCs is presented [1]. It is well known [2] that the major limitation to high linearity of such devices is due to mismatch in the unity elements of the inter-stage MDAC. The linearity of these elements is also critical in achieving harmonic distortion specifications, especially for the first stage of the pipeline. Traditionally, there are several approaches to improve the accuracy of the MDAC. They can broadly be lumped into two categories: Analog element calibration [3], [4], [5] and digital calibration [6], [7]. Analog element calibration or trim corrects the ADC by adjusting the elements in the analog domain. It has two main drawbacks. First, for the case of one-time element trim [4], variations in matching with temperature, power supply fluctuation, aging and so on may degrade the calibration. Second, techniques such as laser trimming or fuse blowing not only add significantly to the cost of an IC but they may not readily scale to modern process technologies. In digital calibration, the

analog errors are measured and digitized and subsequently subtracted from the converter's raw digital output. A common limitation of power up digital calibration [6] is that in order to determine the converter's errors, its operation must be interrupted so that known inputs can be applied. A major limitation of other digital calibration schemes is that they use a separate ADC to digitize the errors. For example, the scheme in [8] employs a separate sigma-delta ADC to quantize the analog errors.

2. PROPOSED METHOD

The main subject matter presented in this paper dwells on how to sequentially auto-extract element MDAC mismatch in background in order to perform digital calibration. This method employs an extra element in the MDAC and a master reference one. An extra element is included so that while another element is under calibration, the rest of the elements continue performing normal A/D operation without interruption. Each unity element (including the extra one) is sequentially placed in calibration mode. This can easily be implemented with a clocked shift register. Mismatch between the selected element and the reference is then digitally extracted and stored in an addressable digital memory from which the INL at each code can be obtained. This INL is then subtracted from the overall converter output to perform calibration. A look-up table whose address is the output of the sub-ADC of the stage under calibration provides the value to be subtracted. Each calibration session requires a relatively large number of clock periods; however, this is not a limit: the mismatch being measured is a static error or it drifts very slowly due to environmental fluctuations.

To be more precise, Fig.1 a) shows a single-ended version of a switched capacitor residue generator incorporating a 2-bit DAC as commonly used in a conventional pipeline. During phase 1, all the capacitors sample the input signal. During phase 2, by proper control of three switches, one capacitor is connected around the op-amp and the rest are switched to the appropriate reference voltages. The capacitors $C_{u,1}$, $C_{u,2}$, $C_{u,3}$ and $C_{u,4}$ are nominally

equal. Assuming that $C_{u,4}$ is connected in feedback, the generated residue is,

$$V_{Res} = \frac{1}{C_{u,4}} \{ (C_{u,1} + C_{u,2} + C_{u,3} + C_{u,4}) \cdot V_{in} - C_{u,1}V_{R,1} - C_{u,2}V_{R,2} - C_{u,3}V_{R,3} \} \quad (1)$$

where $V_{R,1}$, $V_{R,2}$, $V_{R,3}$, are the reference voltages applied to $C_{u,1}$, $C_{u,2}$ and $C_{u,3}$ during phase 2 respectively.

Figs. 1a) and b)– Conventional and modified 2-bit switched capacitor residue generator respectively.

Fig. 1 (b) shows a modified version suitable for this method. We have an additional capacitor $C_{u,5}$ and reference capacitor C_{ref} . The capacitance in the calibration mode is switched between V_{ref} and $-V_{ref}$ with a clocking scheme complementary to the one used for C_{ref} while the other capacitors operate exactly as the ones in the conventional counterpart. Assuming that $C_{u,5}$ is in calibration mode and that it is charged to V_{ref} during the phase 1 (C_{ref} is meanwhile being charged at $-V_{ref}$). The residue voltage becomes,

$$V'_{Res} = \frac{1}{C_{u,4}} \{ (C_{u,1} + C_{u,2} + C_{u,3} + C_{u,4}) \cdot V_{in} - C_{u,1}V_{R,1} - C_{u,2}V_{R,2} - C_{u,3}V_{R,3} + (C_{u,5} - C_{ref}) \cdot V_{Ref} \} \quad (2)$$

This is the conventional residue voltage plus a term that depends on the mismatch between $C_{u,5}$ and C_{ref} . If $C_{u,5}$ is in calibration mode and is charged at $-V_{ref}$ during phase 1 the sign of the additional term is reversed. The process would then sequentially cycle through all the capacitors. This would happen without interrupting the normal operation of the converter. Equation (2) can also be expressed as,

$$V'_{res} = V_{res} \pm \frac{(C_{u,5} - C_{ref}) \cdot V_{ref}}{C_{u,4}} \quad (3)$$

Figs. 2 (a) and (b) presents the current-mode counterpart of the conventional and modified 2-bit residue generator. Four nomi-

nally equal current generators switch towards the positive and negative inputs of the fully differential operational amplifier. Those generators with the two sinks equal to $2I_u$ make the DAC. The modified structure has an extra unity current sink and the reference generator I_{ref} . The switching scheme controlling the reference generator and the unity element under calibration is such that the two currents are injected on the same input terminal. By inspection of the circuit it follows that,

Figs. 2 a) and b) – Conventional and modified 2-bit current mode residual generator respectively.

$$V'_{Res} = V_{Res} \pm (I_{ref} - I_{u,5}) \frac{R_1 + R'_1}{2} \quad (4)$$

Therefore, the modified schemes of Fig. 1(b) and Fig. 2(b) or their extension to more bits are capable of superposing to the conventional residue signal a contribution proportional to the mismatch between a reference element and the element in the calibration mode. The sign of the mismatch contribution can be made positive or negative, depending on the clocking control scheme used. This feature is later exploited to control the mismatch term with a random bit stream.

3. EXTRACTION OF MISMATCH SIGNAL

The output of the modified version of the residue generator can be generalized as,

$$Y'_{res} = Y_{res} + (2X_{mod} - 1)\Delta U \cdot K \quad (5)$$

where X_{mod} is a control bit that determines the sign of the additional DAC mismatch term ΔU and K is assumed to be a gain fac-

tor. The additional contribution modifies the digital output of the pipeline as,

where x_{in} is the input signal, $\mathcal{E}_Q$ is the quantization error, $\varepsilon_{dac,i}$ is the residual error in the DAC elements and $\varepsilon_{dac,k}$ is the error (mis-match) in the k th DAC element under calibration. If the input signal is busy enough to verify the approximation of $\mathcal{E}_Q$ as white noise, the spectrum of the digital output is given by the spectrum of the input signal, the quantization noise, the contribution of $\varepsilon_{dac,i}$ and the mismatch $\varepsilon_{dac,k}$ modulated by a ± 1 signal controlled by X_{mod} .

constant signal; after the scrambling, which is controlled by the `b_sc` bit, the mismatch is added to the input. The quantizer (10 bit resolution in this case) models the pipeline ADC. Since the quantizer does not foresee any delay, the scrambler uses the same control bit `b_sc`. In a real pipeline ADC the conversion process introduces latency. In that case it would be necessary to apply the same latency on `b_sc`.

Fig. 3 – Simulink diagram of the simulation system.

Fig. 4 – Simulink model of the b_sc generator.

The calibration algorithm measures the actual mismatch with a fractional accuracy of,

$$\frac{\Delta x}{n \cdot m} \quad (11)$$

where Δx is the difference between the actual and extracted value, m is the actual mismatch and n is the number of samples (i.e. clock cycles) used to calculate the average. Therefore the accuracy is inversely proportional to $n \cdot m$, an important result. Fig. 5 shows a typical simulation result of the accumulated values. Fig. 6 shows the zoomed-in plot after $6.5e5$ time points. A mismatch at 12 bit level (i.e., 2^{-12}), typical of modern scaled state of the art technologies is assumed. Following equation (11), the calibration algorithm computes the value within an accuracy of $\pm 4 / (6.5e5 \cdot 2^{-12}) = \pm 0.02520$, an improvement of 5.31 bits, thus

Fig. 5 – Mismatch measurement simulation plot.

Fig. 6 – Zoomed-in plot of simulation.

theoretically achieving calibration to $(12+5.31) = 17.31$ bits. In some cases the distance between the ideal and the actual result can become ± 10 . This would lead to a lower accuracy with respect to the above given figure. Effects of digital truncation error have not been included. We have applied the method to 8 different MDAC mismatch situations that cause non-linearity. The worst causes a SFDR of 78dB for a -6dBFS input. The correction with $6.5e5$ clock-cycles improved the SFDR by 24 dB.

The additional circuits required include shift registers, accumulators, clock generator, RAM memory and random number generator. No extra dynamic range burden is imposed on the pipelined converter.

5. CONCLUSION

The technique presented in this paper enables a precise digital measurement of the MDAC response and performs digital background auto-calibration on the pipelined ADC. It employs the intrinsic pipelined converter itself, thus little additional analog circuitry is required; complexity is transferred to the digital domain, a proposition well suited to implementation in modern scaled technologies that tend to include software programmable DSPs which can easily perform the operations of digital calibration. The calibration accuracy depends on the number of clock cycles used for each session. The fundamental limitation would emerge from the thermal noise floor and sampling jitter or aperture uncertainty present in the electronic circuit.

6. REFERENCES

- [1] Franco Maloberti, Martin Kinyua, "Continuous digital background calibration in pipelined ADC architecture," USA patent, filed December 2003.
- [2] S. H. Lewis, "Video-rate analog-to-digital conversion using pipelined architectures," Memo. No. UCB/ERL M87/90, Electronics Research Laboratory, UC Berkeley, Nov. 1987.
- [3] J. M. Ingino, B. A. Wooley, "A continuously calibrated 12-b 10MS/s, 3.3-V A/D Converter," IEEE JSSC, pp. 1920-1931, Dec 1998.
- [4] C. Moreland, et al "A 14-bit 100- Msamples/s Subranging ADC," IEEE JSSC, vol.35, No. 12, December 2000.
- [5] D. W. J. Groenvelde et al., "A self-calibration Technique for monolithic High-Resolution D/A Converters," IEEE JSSC Vol. SC-24, pp 1517-1522, Dec. 1989.
- [6] A. Karanicolas, H. Lee, K. Bacrania, "A 15-bit-Msample/s digitally self-calibrated pipeline ADC," IEEE JSSC, Vol 28, pp. 1207-1215, Dec. 1993.
- [7] S. Hisano, S. Sapp, "A 16-Bit 20MSPS CMOS pipeline ADC with Direct INL Detection Algorithm," IEEE CICC pp. 417-420, 2003.
- [8] T. Shu, B. Song, and K. Bacrania, "A 13-b 10-Msamples/s ADC digitally calibrated with oversampling delta-sigma converter," IEEE JSSC, vol. 30, pp. 443-452, April 1995.