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DIGITAL BACKGROUND AUTO-CALIBRATION OF DAC NON-LINEARITY
IN PIPELINED ADCs

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ABSTRACT

In this paper, a digital background auto-calibration method that computes mismatch between the elements of the inter-stage Multiplying-Digital-to-Analog Converter (MDAC) as commonly employed in pipelined Analog-to-Digital Converters (ADCs) and then applies a linearizing algorithm in the digital domain is described. The calibration does not interrupt the normal operation of the ADC and is performed periodically, thus inherently able to track changes in the operating conditions of the device, a major limitation of one-time calibration approaches. This scheme requires an extra MDAC element and a reference element. The MDAC mismatch is digitized by the succeeding stages of the pipeline and subsequently digitally extracted. The accuracy of the calibration algorithm depends on the number of clock periods used for each calibration session. Longer sessions lead to better accuracy with the trade-off being additional digital circuitry. System simulation results demonstrate validity of the approach.

1. INTRODUCTION

In this paper, a method to calibrate pipelined ADCs is presented [1]. It is well known [2] that the major limitation to high linearity of such devices is due to mismatch in the unity elements of the inter-stage MDAC. The linearity of these elements is also critical in achieving harmonic distortion specifications, especially for the first stage of the pipeline. Traditionally, there are several approaches to improve the accuracy of the MDAC. They can broadly be lumped into two categories: Analog element calibration [3], [4], [5] and digital calibration [6], [7]. Analog element calibration or trim corrects the ADC by adjusting the elements in the analog domain. It has two main drawbacks. First, for the case of one-time element trim [4], variations in matching with temperature, power supply fluctuation, aging and so on may degrade the calibration. Second, techniques such as laser trimming or fuse blowing not only add significantly to the cost of an IC but they may not readily scale to modern process technologies. In digital calibration, the analog errors are measured and digitized and subsequently subtracted from the converter’s raw digital output. A common limitation of power up digital calibration [6] is that in order to determine the converter’s errors, its operation must be interrupted so that known inputs can be applied. A major limitation of other digital calibration schemes is that they use a separate ADC to digitize the errors. For example, the scheme in [8] employs a separate sigma-delta ADC to quantize the analog errors.

2. PROPOSED METHOD

The main subject matter presented in this paper dwells on how to sequentially auto-extract element MDAC mismatch in background in order to perform digital calibration. This method employs an extra element in the MDAC and a master reference one. An extra element is included so that while another element is under calibration, the rest of the elements continue performing normal A/D operation without interruption. Each unity element (including the extra one) is sequentially placed in calibration mode. This can easily be implemented with a clocked shift register. Mismatch between the selected element and the reference is then digitally extracted and stored in an addressable digital memory from which the INL at each code can be obtained. This INL is then subtracted from the overall converter output to perform calibration. A look-up table whose address is the output of the sub-ADC of the stage under calibration provides the value to be subtracted. Each calibration session requires a relatively large number of clock periods; however, this is not a limit: the mismatch being measured is a static error or it drifts very slowly due to environmental fluctuations.

To be more precise, Fig.1 a) shows a single-ended version of a switched capacitor residue generator incorporating a 2-bit DAC as commonly used in a conventional pipeline. During phase 1, all the capacitors sample the input signal. During phase 2, by proper control of three switches, one capacitor is connected around the op-amp and the rest are switched to the appropriate reference voltages. The capacitors \(C_{u,1}, C_{u,2}, C_{u,3}\) and \(C_{u,4}\) are nominally
equal. Assuming that \( C_{u,4} \) is connected in feedback, the generated residue is,
\[
V_{\text{res}} = \frac{1}{C_{u,4}} \left( (C_{u,1} + C_{u,2} + C_{u,3} + C_{u,4}) V_{\text{in}} - \right.
- \left. C_{u,1} V_{R,1} - C_{u,2} V_{R,2} - C_{u,3} V_{R,3} \right)
\]
where \( V_{R,1}, V_{R,2}, V_{R,3} \) are the reference voltages applied to \( C_{u,1}, C_{u,2} \) and \( C_{u,3} \) during phase 1 respectively.

\[
\text{Figs. 1 a) and b) – Conventional and modified 2-bit switched capacitor residue generator respectively.}
\]

Fig. 1 (b) shows a modified version suitable for this method. We have an additional capacitor \( C_{u,5} \) and reference capacitor \( C_{\text{ref}} \). The capacitance in the calibration mode is switched between \( V_{\text{ref}} \) and \( -V_{\text{ref}} \) with a clocking scheme complementary to the one used for \( C_{\text{ref}} \) while the other capacitors operate exactly as the ones in the conventional counterpart. Assuming that \( C_{u,5} \) is in calibration mode and that it is charged to \( V_{\text{ref}} \) during the phase 1 (\( C_{\text{ref}} \) is meanwhile being charged at \( -V_{\text{ref}} \)). The residue voltage becomes,
\[
V'_{\text{res}} = \frac{1}{C_{u,4}} \left( (C_{u,1} + C_{u,2} + C_{u,3} + C_{u,4}) V_{\text{in}} - C_{u,1} V_{R,1} - 
- C_{u,2} V_{R,2} - C_{u,3} V_{R,3} + (C_{u,5} - C_{\text{ref}}) V_{\text{ref}} \right)
\]
This is the conventional residue voltage plus a term that depends on the mismatch between \( C_{u,5} \) and \( C_{\text{ref}} \). If \( C_{u,5} \) is in calibration mode and is charged at \( -V_{\text{ref}} \) during phase 1 the sign of the additional term is reversed. The process would then sequentially cycle through all the capacitors. This would happen without interrupting the normal operation of the converter. Equation (2) can also be expressed as,
\[
V'_{\text{res}} = V_{\text{res}} \pm \frac{(C_{u,5} - C_{\text{ref}})}{C_{u,4}} V_{\text{ref}}
\]
Figs. 2 (a) and (b) presents the current-mode counterpart of the conventional and modified 2-bit residue generator. Four nominally equal current generators switch towards the positive and negative inputs of the fully differential operational amplifier. Those generators with the two sinks equal to \( 2I_{\text{in}} \) make the DAC. The modified structure has an extra unity current sink and the reference generator \( I_{\text{ref}} \). The switching scheme controlling the reference generator and the unity element under calibration is such that the two currents are injected on the same input terminal. By inspection of the circuit it follows that,
\[
V' \text{ Re} s = V_{\text{Re} s} \pm (I_{\text{ref}} - I_{u,5}) \frac{R_1 + R'_1}{2}
\]
Therefore, the modified schemes of Fig. 1(b) and Fig. 2(b) or their extension to more bits are capable of superposing to the conventional residue signal a contribution proportional to the mismatch between a reference element and the element in the calibration mode. The sign of the mismatch contribution can be made positive or negative, depending on the clocking control scheme used. This feature is later exploited to control the mismatch term with a random bit stream.

3. EXTRACTION OF MISMATCH SIGNAL

The output of the modified version of the residue generator can be generalized as,
\[
y'_{\text{res}} = y_{\text{res}} + (2X_{\text{mod}} - 1)\Delta U \cdot K
\]
where \( X_{\text{mod}} \) is a control bit that determines the sign of the additional DAC mismatch term \( \Delta U \) and \( K \) is assumed to be a gain fac-
Then modulating \( y_{\text{out}} = x_{\text{in}} + \varepsilon_Q + \sum_{i \neq k} \varepsilon_{\text{dac},i} + (2X_{\text{mod}} - 1)\varepsilon_{\text{dac},k} \) (6)

where \( x_{\text{in}} \) is the input signal, \( \varepsilon_Q \) is the quantization error, \( \varepsilon_{\text{dac},i} \) is the residual error in the DAC elements and \( \varepsilon_{\text{dac},k} \) is the error (mis-match) in the \( k \)th DAC element under calibration. If the input signal is busy enough to verify the approximation of \( \varepsilon_Q \) as white noise, the spectrum of the digital output is given by the spectrum of the input signal, the quantization noise, the contribution of \( \varepsilon_{\text{dac},i} \) and the mismatch \( \varepsilon_{\text{dac},k} \) modulated by a \( \pm 1 \) signal controlled by \( X_{\text{mod}} \).

Then modulating \( y_{\text{out}} \) with \( (2X_{\text{mod}} - 1) \) and averaging the result over a long number of clock periods yields,

\[
< y_{\text{out}}(2X_{\text{mod}} - 1) >= < x_{\text{in}}(2X_{\text{mod}} - 1) > + < \varepsilon_Q(2X_{\text{mod}} - 1) > + \sum_{i \neq k} \varepsilon_{\text{dac},i} (2X_{\text{mod}} - 1) + \varepsilon_{\text{dac},k}
\] (7)

The contribution of \( \varepsilon_Q \) should vanish because the modulation of white noise with any signal produces white noise and its average over a long number of clock periods tends to zero. Observe that the modulation of the mismatch term makes the sign equal to plus; therefore the operation is equivalent to a synchronous demodulation of \( \varepsilon_{\text{dac},k} \). The goal is to measure \( \varepsilon_{\text{dac},k} \). The result is achieved if the dc components of,

\[
x_{\text{in}}(2X_{\text{mod}} - 1) \quad \text{and} \quad \varepsilon_{\text{dac},k}(2X_{\text{mod}} - 1)
\] (8)

are negligible with respect to \( \varepsilon_{\text{dac},k} \). This is possible for specific modulation signals \( X_{\text{mod}} \). For example, if the input is band-limited using an out-of-band square-wave modulation the term due to \( X_{\text{in}} \) will vanish. Unfortunately, for Nyquist-rate applications the above mentioned solution is not applicable.

This method uses a special pseudo-random signal bit-stream made by an equal number of 1 and 0. This, as will be seen in the simulation verification brings to zero the three terms,

\[
< x_{\text{in}}(2X_{\text{mod}} - 1) > \quad < \varepsilon_Q(2X_{\text{mod}} - 1) > \quad < \sum_{i \neq k} \varepsilon_{\text{dac},i}(2X_{\text{mod}} - 1) >
\] (9)

Therefore, it results,

\[
<y_{\text{out}}(2X_{\text{mod}} - 1) >= \varepsilon_{\text{dac},k}
\] (10)

### 4. SIMULATION RESULTS

Simulink simulations have verified the proposed method. Fig. 3 shows the basic block diagram for the case of simulating extraction of a single \( k \)th DAC element mismatch. The mismatch is a constant signal; after the scrambling, which is controlled by the \( b_{\text{sc}} \) bit, the mismatch is added to the input. The quantizer (10 bit resolution in this case) models the pipeline ADC. Since the quantizer does not foresee any delay, the scrambler uses the same control bit \( b_{\text{sc}} \). In a real pipeline ADC the conversion process introduces latency. In that case it would be necessary to apply the same latency on \( b_{\text{sc}} \).

![Simulink diagram of the simulation system.](image)

**Fig. 3 – Simulink diagram of the simulation system.**

The generation of the scrambling bit-stream must be random, with white noise spectrum and the same average number of ones and zeros. Fig. 4 shows the block diagram used in simulations. It uses a band-limited white noise generator whose sign determines a random bit-stream. The next section controls the running balance between 1 and 0. If the balance exceeds the high threshold or is lower than the low threshold a 0 or a 1 respectively replaces the entering bit. The use of running balance control is essential for the operation: the algorithm for generating random numbers and the circuits that provide pseudo-random sequences do not ensure that the number of positive outputs equals the number of negative outputs within an arbitrary calibration time period. Simulation show that the spectrum of the bit-stream at the output of the circuit in Fig. 4 is, as desired, white. The thresholds were set to 4 and –4.

The input signal generator used for simulations is a combination of four generators, a band-limited noise (with a seed different from the one used in the block of Fig. 3), two sine-wave generators and an offset. This permits us to investigate different input situations; namely an offset, random signals and sinusoidal waves.
The calibration algorithm measures the actual mismatch with a fractional accuracy of,

$$\frac{\Delta x}{n \cdot m}$$ \hspace{1cm} (11)

where $\Delta x$ is the difference between the actual and extracted value, $m$ is the actual mismatch and $n$ is the number of samples (i.e. clock cycles) used to calculate the average. Therefore the accuracy is inversely proportional to $n \cdot m$, an important result. Fig. 5 shows a typical simulation result of the accumulated values. Fig. 6 shows the zoomed-in plot after 6.5e5 time points. A mismatch at 12 bit level (i.e., $2^{-12}$), typical of modern scaled state of the art technologies is assumed. Following equation (11), the calibration algorithm computes the value within an accuracy of $\frac{-4}{(6.5e5 \cdot 2^{-12})} = 0.02520$, an improvement of 5.31 bits, thus theoretically achieving calibration to $(12 + 5.31) = 17.31$ bits. In some cases the distance between the ideal and the actual result can become $\frac{1}{10}$. This would lead to a lower accuracy with respect to the above given figure. Effects of digital truncation error have not been included. We have applied the method to 8 different MDAC mismatch situations that cause non-linearity. The worst causes a SFDR of 78dB for a –6dBFS input. The correction with 6.5e5 clock-cycles improved the SFDR by 24 dB.

The additional circuits required include shift registers, accumulators, clock generator, RAM memory and random number generator. No extra dynamic range burden is imposed on the pipelined converter.

5. CONCLUSION

The technique presented in this paper enables a precise digital measurement of the MDAC response and performs digital background auto-calibration on the pipelined ADC. It employs the intrinsic pipelined converter itself, thus little additional analog circuitry is required; complexity is transferred to the digital domain, a proposition well suited to implementation in modern scaled technologies that tend to include software programmable DSPs which can easily perform the operations of digital calibration. The calibration accuracy depends on the number of clock cycles used for each session. The fundamental limitation would emerge from the thermal noise floor and sampling jitter or aperture uncertainty present in the electronic circuit.

6. REFERENCES


