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A HIGH SPEED AND LOW POWER CMOS CURRENT COMPARATOR FOR PHOTON COUNTING SYSTEMS

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ABSTRACT

In this paper a CMOS current comparator for a photon counting system is proposed. The device can be used in satellite acquisition systems for UV free space studies. The circuit features a 4 bit programmable threshold, to avoid wrong counting due to the dark current of the detector and a four bits counter, to perform a post acquisition analysis. The specifications of the system are based on the characteristics of the HAMAMATSU H7546 multianode photomultiplier. The circuit, implemented in a 0.35 μ m CMOS technology, consumes less than 1 mW from a 3.3 V power supply and can operate properly up to 70° C.

1. INTRODUCTION

The Ring Imaging Cherenkov (RICH) devices are, nowadays, the most important sensors to analyze charged particles, generated from the high energy nuclear and subnuclear interaction. When a charged particle is emitted in radioactive decay with velocity greater than c/n (the speed of light in the medium), where c is the speed of light in vacuum and n is the index of refraction of the medium (radiator), a “shock wave” of photons is generated in the blue light range, analogous to the sonic boom of a jet flying faster than the speed of sound. By transducing the light produced in an electrical signal with a sensor and counting with a suitable read-out circuitry the incident photons, it is possible to derive some information about the particles under observation. The photomultiplier is the device most commonly used for transducing the emitted light in an electrical signal in this kind of application, because of its high gain.

Applications of the RICH sensors include:

- satellite acquisition systems for UV free space studies;
- detection of high energy elementary particles in physics;
- assaying of P-32, which in a water solution with a liquid scintillator has a detectable Cherenkov emission in nuclear medicine.

The detection system where the circuit presented in this paper has to operate is shown in Fig. 1. The system includes a ma-

Figure 1. Simplified block diagram of the Cherenkov effect detector with the electronic system connected on the rear of the sensor

trix of 8×8 elements, consisting each of 8×8 photomultipliers, and the electronic read-out circuit. The read-out circuit consists of 64 chips, each including 64 instances of the proposed circuit, which are used to count the events occurring in the whole matrix of photomultipliers. To reduce as much as possible the effect of the parasitic capacitance of the connection between detector, board and electronics, bump bonding is used.

The proposed circuit is directly connected to the detector; the input signal is a poissonian current with rise time equal to 2 ns, pulse width equal to 5 ns and maximum operating frequency equal to 100 MHz. To avoid wrong counting, due to the dark current of the sensors, a 4 bit programmable threshold is used. The number of events occurred is stored in a four bit counter. The delay introduced by the whole chain has to be lower than 5 ns. Since the considered RICH system will be used on a satellite our attention was focused on developing a very low power system. Indeed, the maximum power budget allowed for each channel of the read-out electronics is about 1 mW.

2. SYSTEM OPERATION

The considered detection system will be used to perform experiments requiring very fast acquisitions. The most critical block of the whole read-out circuit is, therefore, the current comparator, that is placed at the input of the analog chain. The current comparator designed for this system, can be used in any other application that requires very fast and low power current comparison.

The specifications of the system are based on the characteristics of the HAMAMATSU H7546 photomultipliers. In order to count the number of photons that hit the photomultiplier, the current pulses produced at the input of the read-out circuit have to be compared with a programmable threshold level, transformed in logic pulses and then counted.

More in detail, when an event occurs, the charged particle flies through a radiator and, because of the Cherenkov effect, light is emitted in the visible or UV spectrum. The light excites the photomultiplier, that produces an output current with poissonian distribution, which represents the input signal of the read-out circuit. If this current is higher than the threshold level, a digital signal is generated. This signal is used to increment the value stored in a counter which hence provides the number of events occurred. In literature two possible structures are proposed to detect the output current of a photomultiplier (Fig. 2):

- using a transimpedance stage and a voltage comparator[1];
- using a current comparator[2];

Figure 2. Simplified schematics of the current comparators proposed in literature

In the circuit shown in Fig. 2a, the current which flows out from the sensor is transformed by a resistor into a voltage, which is then compared with a programmable threshold by means of voltage comparator. The main problem of this technique is that the presence of the input resistor introduces a trade-off between sensitivity and speed. Indeed, if the input resistance is large it is possible to achieve a good sensitivity, but the inevitably large time constant produced by the resistor itself together with the capacitance of the detector limits the operating speed [3].

The circuit shown in Fig. 2b, by contrast, exploits a cascode current mirror to read-out the current pulse. The difference between the threshold current and the signal current is then transformed into a voltage by the cascode output resistance. To increase the amplitude of the output voltage, some CMOS

inverters are added at the output. The worst problem of this approach is that the output resistance of the cascode structure is extremely high and, therefore, because of the input capacitance of the following stages, the bandwidth of the comparator is intrinsically small, thus making this circuit unsuitable for high speed applications [4].

In this paper we propose an innovative technique to detect the current of the photomultiplier. The key idea in the proposed circuit is to reduce the input resistance, using a local feedback loop [5]. In this way the cut off frequency associated with the input node is increased, and therefore, the circuit becomes suitable for high speed applications.

The block diagram of the proposed acquisition chain is shown in Fig. 3. The photomultiplier current and the threshold current are subtracted at the input and injected in a very low impedance node (thanks to the local negative feedback loop). This current is then transformed into a voltage and amplified. The resulting voltage pulse is used to drive a 4-bit counter which stores into a register the number of the high energy particles arrived. This value is then delivered to the external acquisition system of the RICH apparatus. The complete read-out circuit consists of 64 instances of the above mentioned acquisition channel, which share the same threshold current, controlled by a 4-bit current DAC. The data for programming the acquisition channels and the output data recorded are transmitted serially.

Figure 3. Block diagram of the proposed acquisition chain

3. CIRCUIT DESCRIPTION

The proposed acquisition chain can be divided in three basic building blocks. The core of the analog chain is the current comparator. The schematic of this circuit is shown in Fig. 4. The input section consists of two common gate MOS transistors (M_1 and M_2) which can accept input currents of both polarities. Transistors M_3 and M_4 are used as level shifters to properly bias the input transistors, with $10\ \mu\text{A}$ of current. To achieve very high speed of operation, the circuit exploits, as mentioned above, a local negative feedback loop (M_5 - M_8), which reduces the input resistance and hence the time constant (τ) associated with the input node. The feedback loop consists of a feedback amplifier which senses the voltage at the input node and adjusts the voltage at the source of M_3 and M_4 (and hence the current flowing in M_1 and M_2) in order to maintain the input node voltage equal to the reference voltage V_{ref} .

With this solution, the value of τ is given by

$$\tau = R_{IN} C_{detector}, \quad (1)$$

with

Figure 4. Schematic of the current comparator

$$R_{IN} = \frac{1}{(1 + A_0)(g_{m1} + g_{m2})} \quad (2)$$

where A_0 is the gain of the feedback amplifier (M_5 - M_8), while g_{m1} and g_{m2} denote the transconductances of M_1 and M_2 , respectively. The feedback amplifier is a simple single ended differential pair with active load. The main characteristic of this amplifier are summarized in Tab. 1.

Parameter	Value
DC Gain	36 dB
Bandwidth (-3 dB)	131 MHz
Phase Margin	84°

Table 1. Performances of the feedback amplifier

For this kind of application it is very important that the amplifier achieves a very large bandwidth and a good phase margin, while the gain can be relatively low. The signal at the output of the feedback amplifier, besides closing the feedback loop, is also amplified with two digital inverters, used as open loop gain stages, and delivered to the counter [5]. The problem of this approach, is that the optimum bias point of the inverters is sensitive to the technological spread of the component parameters and to the DC offset of the previous stage. However this solution achieves a very high gain and very high speed. As well known, the gain of this stage is given by

$$A_0 = \left(\frac{1}{r_{DS_p}} + \frac{1}{r_{DS_n}} \right) \cdot (g_{m_p} + g_{m_n}) \quad (3)$$

Using symmetrical inverters, the reference voltage V_{ref} is binded to $V_{dd}/2$, biasing properly all the stages in the current comparator. In designing the circuit, particular care has been taken in minimizing the capacitive load of all the nodes, in order to achieve the maximum possible speed.

The current DAC used to produce the threshold current consists of 16 current mirrors, selected by nMOS switches, as

Figure 5. Schematic of the 4-bit DAC for producing the threshold current

achieve a larger output resistance, that allows us to minimize the linearity errors, since the DAC is connected to a low impedance node. The full scale current of the DAC is equal to 12.2 A, which corresponds to the current produced by the photomultiplier in response to two incident photons. With 16 steps, the value of DAC's least significant bit (LSB) is equal to 0.81 A.

The last building block of the system is the asynchronous counter, whose schematic is shown in Fig. 6. The circuit is re-

Figure 6. Schematic of the 4-bit counter

alized with 4 standard cell flip-flops and besides the input signal, it foresees also

- the GTU_RESET signal to clear the memory of the counter;
- the INHIBIT signal to avoid counter update during the data transfer.

During acquisition the INHIBIT signal is high, thus enabling the counter. When the INHIBIT signal goes low, the counter holds the value and waits to transfer the data to the external acquisition system. When the data has been read, the GTU_RESET signal is used to restart the acquisition. We used an asynchronous counter because it is very simple and, for this application, the synchronization problem is negligible. The most critical transition for this counter, which occurs from 0001 to 1000, is completed in less than 3 ns.

4. SIMULATION RESULTS

The system has been extensively simulated using a 0.35 μm CMOS process, in order to demonstrate the effectiveness of the proposed solution. The current comparator has been stimulated using a poisson-like current. This waveform has been implemented with 0.4 ns resolution in time for 10 ns. The circuit was simulated both with a single shot and with a train of pulses replicated at 100 MHz frequency. Fig. 7 shows the re-

Figure 7. Response of the circuit to a single shot event

sponse of the current comparator in typical conditions (27°C) to a single shot event occurring after 50 ns. The response time of the circuit is about 4 ns. Moreover, to validate the structure for satellite applications, a parametric analysis over temperature has been performed, as shown in Fig. 8. The circuit operates properly until 70°C. For higher temperatures the response time becomes larger than the specification. If the temperature becomes higher than 80°C errors in counting degrade the system performance. These errors are due to the fact that the optimum bias voltage of the first inverter becomes too large and the gain of the chain drops. Nevertheless, the circuit achieves a remarkable response time (less than 5 ns) in the temperature range from 0°C to 70°C with a power consumption of 990 μW from a 3.3 V power supply, as reported in Tab. 2.

Figure 8. Response of the system to a single shot event at different temperatures

Parameter	Value
Response time	5 ns
Temperature range	0° to 70° C
Power consumption	990 μW
Power supply	3.3 V
Technology	0.35 μm CMOS

Table 2. Performance summary of the proposed circuit

5. CONCLUSIONS

In this paper we present a novel acquisition chain for photon counting applications. The core of the system is a high-speed, low-power current comparator. The simulations confirm that a response time as low as 5 ns can be achieved with less than 1 mW of power consumption. The solution proposed is suitable for detecting charge particle emissions, due the Cherenkov effect in satellite applications. The circuit works up to 70°C, and can detect 10^8 events/s.

REFERENCES

- [1] G. Palmsano, G. Palumbo, S. Pennisi, "A CMOS Transresistance Current Amplifier", IEEE ISCAS 1997, Vol 3, pp. 1960-1963, June 1997
- [2] D. Freitas, K. Current, "CMOS Current Comparator Circuit", Electronics Letters, Vol. 19, NO. 17, pp. 695-697, August 1983
- [3] L. Chen, B. Shi, C. Lu, "A Robust High Speed and Low Power Current Comparator Circuit", IEEE APCCAS 2000, pp 147-177, May 2000
- [4] L. Luh, J. Choma, J. Draper, "A High Speed High Resolution CMOS Current Comparator", IEEE ICECS 1999, Vol. 1, pp. 303-306, September 1999.
- [5] H. Lin, J. Huang, S. Wong, "A Simple high-speed low current comparator", IEEE ISCAS 2000, Vol. 2, pp. 713-716, May 2000