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A 0.18μm CMOS SC LOWPASS FILTER FOR BLUETOOTH CHANNEL SELECTION

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ABSTRACT

The integrated circuit design of a switched-capacitor filter for Bluetooth specifications is described. It was based on the optimum allocation of poles and zeros to generate a transfer function with unequal numerator and denominator orders, so that a direct-form structure with reduced number of opamps and low sensitivity to capacitor ratio errors were obtained. It was designed for implementation in the TSMC 0.18 μm CMOS process, using differential OTA structures with a dynamic biasing circuit to reduce power consumption. Layout strategies were carefully considered in order to reduce non-ideal effects. With the aid of a computer program, simulations with the extracted parameters were performed to verify the integrated circuit performance.

1. INTRODUCTION

Having benefitted from improvements in the performance of CMOS operational amplifiers and the availability of high-quality capacitors and switches, switched-capacitor (SC) networks have been extensively employed in analog sampled-data filter realizations. Since the accuracy of such filters relies on the physical parameters of the fabrication process, it is of interest to find low-sensitivity SC filter structures, such that the performance of the integrated circuit implementation will not be compromised by inherently random process variations.

The purpose of this paper is to present the integrated circuit design of a SC filter that satisfies channel selection requirements in Bluetooth radio interface [1], and possesses low-sensitivity to capacitor ratio errors, approximately linear phase and low power consumption. Section 2 describes the basic theoretical concepts of the filtering structure. Design and layout details are considered in Sections 3 and 4, respectively. Post-layout simulation results are shown in Section 5. Concluding remarks are given in Section 6.

2. BASIC CONCEPTS

The integrated circuit described in this paper makes use of the approach described in [2], which in turn is based on the optimum allocation of poles and zeros [3] to generate transfer functions with unequal numerator and denominator orders [4]. As a result, the direct-form SC filter structure can be efficiently combined with designs having a small number of opamps multiplexed in time [5], so that low sensitivity and low power consumption are achieved.

The direct-form structure is in general avoided, specially by analog circuit designers, because the transfer function poles are highly sensitive to variations in the denominator coefficients. However, the approach described in [2] presented a viable alternative to reduce such sensitivities in direct-form SC filters designs. To verify the predicted sensitivity and key theoretical design considerations, a prototype filter was built with discrete switches and opamps for low-frequency operation, but satisfying selectivity specifications similar to those required in Bluetooth applications. Experimental results and design details are shown in [6], along with a discussion regarding the advantages this approach may find over other well-known SC filtering structures commonly applied in practical situations. The results obtained with the prototype filter were in close agreement with the theory, revealing other features such as low power consumption, low capacitance spread and approximately linear-phase frequency response, an issue of particular interest in modern telecommunication systems.

The Bluetooth filter specifications and the resulting SC filter schematic diagram are shown here for convenience. The filter was designed to work at a sampling frequency of 2.5 MHz, with passband and stopband edge frequencies of, respectively, 500 kHz and 750 kHz, passband ripple of 1 dB and stopband attenuation of 60 dB. Since numerator and denominator orders are 8 and 2, respectively, the filter structure is composed of five second-order FIR cells, each of them using only one opamp multiplexed in time, at the expense of five clock phases. Four of the basic cells are in the forward path, implementing the numerator, and one in the feedback path, realizing the denominator. The corresponding block diagram and the final filter structure are depicted in Figs. 1 and 2, respectively. The filter low sensitivity to capacitance ratio variations stems from the fact that its transfer function has only two poles, which are not as close to the unit circle in the z-plane as are the poles of the elliptic transfer function that satisfies the above frequency specifications.

3. DESIGN CONSIDERATIONS

Using a computer-aided program [7], the filter of Fig. 2 was modeled and simulated, exploiting trade-off among close-loop gain, slew-rate and gain-bandwidth product (GB). As a result, the following opamp design requirements were obtained: open-loop gain of 60 dB, GB of 23 MHz and slew-rate of 45 V/μm. Based on these features, the filter was designed for fabrication in a TSMC 0.18 μm CMOS process, with a 1.8 V power supply, using fully-differential folded-cascode OTAs, incorporating a dynamic commo-
mode feedback module [8]. Differential structures are useful in analog IC designs, since they reduce non-ideal effects, such as charge injection and noise, and double the output signal swing.

The OTA was designed considering the worst load case, according to the minimum design requirements presented above. The total current consumption, open-loop gain, phase margin, GB and settling time were, respectively, 157.5 μA, 71 dB, 81.46°, 57.79 MHz and 40 ns. Since the request for low-power consumption is one of the most important features in today’s integrated designs, a dynamic biasing circuit [9] was introduced in the previous OTA structure. The basic idea is to improve the slew-rate and make it possible to lower the current, and consequently reduce power consumption.

The dynamic biasing structure detailed in Fig. 3 consists of one additional differential pair, to monitor the unbalance between the input signals \( V_{in^+} \) and \( V_{in^-} \), and three current sources. If the input signals are balanced, the current \( I \), which is a fraction of the OTA output current, is equally divided between the two transistors, and the voltages \( V_o \) and \( V_b \) are low. On the other hand, when the OTA is in slewing condition and the input voltages are sufficiently unbalanced, the current \( I \) flows entirely through one of the transistors of the additional differential pair, making the related control voltage \( (V_{o} \text{ or } V_{b}) \) go high, to provide the additional current required to improve the slew-rate. It was thus possible to reduce the OTA current consumption down to 78.75 μA, implying in a reduction of about 50% in the power consumption.

4. LAYOUT DETAILS

Because of the modular aspect of the structure of Fig. 2, it was possible to verify the performance of each cell separately, and develop the layout of each cell independently of the other ones, which considerably alleviated the task of identifying and preventing possible faults. To reduce the errors caused by gradient effects in the circuit, such as variations in temperature and in oxide thickness, all transistors were realized as parallel combinations of smaller ones. Transistors belonging to the same current mirror were implemented as multiples of a unitary transistor and interdigitated among themselves to improve matching and equally distribute gradient effects.

The filter coefficients were realized as ratios of capacitors, each one implemented as parallel associations of square unit size capacitors of 0.1 μF, to reduce overetching and fringe parasitic capacitance effects. All the integer capacitor values were chosen to
limit the maximum transfer function coefficient errors to approximately 4 %, and were optimized for the desired output voltage swing. The capacitor values, expressed as integer multiples of the unit capacitor, are listed in Table 1. Their layouts were carefully considered so that the capacitance ratio errors caused parasitic capacitances could be kept as low as 0.1 %, to agree with the sensitivity analyses performed in [6].

Table 1. Capacitor values expressed as integer multiples of the unit capacitor (0.1 pF).

<table>
<thead>
<tr>
<th>Cell 1</th>
<th>Cell 2</th>
<th>Cell 3</th>
<th>Cell 4</th>
<th>Cell 5</th>
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<tbody>
<tr>
<td>C1a</td>
<td>10</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>C1b</td>
<td>10</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>C1c</td>
<td>5</td>
<td>3</td>
<td>8</td>
<td>3</td>
</tr>
<tr>
<td>C1d</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>C1e</td>
<td>2</td>
<td>-</td>
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<td>-</td>
</tr>
<tr>
<td>C2a</td>
<td>4</td>
<td>5</td>
<td>9</td>
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<tr>
<td>C2b</td>
<td>-</td>
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</tr>
<tr>
<td>C2c</td>
<td>8</td>
<td>3</td>
<td>4</td>
<td>3</td>
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<tr>
<td>C1f</td>
<td>1</td>
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<td>C1g</td>
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The switches were designed for complementary operation, in order to use the entire range 0-1.8 V, with parallel associations of small transistors to improve matching. Also, dummy elements were employed to reduce charge injection effects. The layouts of the switches were carefully planned, so as to avoid crossings between the signal and the clock phases, and hence prevent crosstalk between analog and digital signals.

To drive the output PADS and passive probe, the output buffer of Fig. 5 was designed in a fully-differential folded-cascode structure for a 15 pF load, and its performance was similar to the other OTAs designed.

Considering all the details presented and also following design strategies to separate the analog signals from the digital ones, it was possible to develop a modular design, based on small cells, thereby taking the advantages of the differential architectures. As a result, the filter layout depicted in Fig. 6 is completely symmetric.

The filter described in the previous sections was simulated in a CADENCE platform, using parameters extracted from the filter layout to verify the IC predicted performance. Shown in Fig. 7, the ideal and simulated frequency responses are in close agreement. The small shift in one of the zeros to a higher frequency is caused by unavoidable parasitic capacitances. The minimum stopband attenuation of 60 dB is nonetheless achieved. The total chip dimensions are 1.510 mm x 0.778 mm and it will be encapsulated in a 28-pin leaded chip carried case. Its maximum estimated power consumption is 0.85 mW.

5. POST-LAYOUT SIMULATIONS

Fig. 5. Output buffer schematic.

Fig. 6. Final layout of the chip.
6. CONCLUDING REMARKS

The integrated circuit implementation of a filter for channel selection specifications in Bluetooth radio interface was described in this work. The theoretical filter design was based on optimum allocation of poles and zeros, leading to designs with different numerator and denominator orders. Its structure comprised second-order direct-form FIR cells, each of them implemented with only one time-multiplexed opamp, giving the implementation a useful modular aspect. The basic design parameters requirements were identified and fully-differential folded-cascode OTAs were designed to fulfill the specifications. Aiming at power consumption reduction, a dynamic biasing structure was incorporated to the OTA design.

The filter was designed for fabrication in a TSMC 0.18 μm CMOS technology. Layout techniques were applied to reduce non-ideal effects, such as charge injection, parasitic capacitances and crosstalk between analog and digital signals. Details of the layout design, taking advantages of differential architectures, were described. Post-layout computer-aided simulations were performed, to verify the structure low-sensitivity and low power consumption.

ACKNOWLEDGEMENTS

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7. REFERENCES


