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A 14-BIT 20-MSAMPLES/S PIPELINED A/D CONVERTER WITH HIGH SLEWING AMPLIFIER

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Abstract - This paper describes a 14-bit 20MSPS switched-capacitor pipelined ADC designed in a complementary SiGe/SOI bipolar process. It features an input-to-output class A/B operational amplifier designed to drive large sampling capacitors of 10pF without consuming excessive power. Prototype implementation exhibits measured INL of ±2.0 LSB, DNL of ±0.5 LSB, SNR of 73 dB and SFDR of 85 dB with a 2MHz input signal. Analog power dissipation at lowest amplifier bias setting is 390mW with 5V supply.

Keywords: A/D and D/A Conversion.

1. INTRODUCTION

The recent trend in VLSI system integration is the continued shift from signal processing in the analog domain to signal processing in the digital domain. This is driven by the scaling of advanced semiconductor processes and the ability to perform complex operations in the digital domain using DSPs, which can easily be reconfigured via software. However, this trend has placed challenging specifications on the ADC, which straddles the interface between the analog and digital domains. Low power yet high dynamic range designs are the preferred trend in order to ease thermal management and reduce system footprint [1]. ADCs for applications such as wideband digital communication systems need excellent SNR to avoid losing the weak signal in the quantization or thermal noise. They also require high spurious free dynamic range (SFDR) to avoid masking the weak signal with distortion artifacts from the stronger signal. These ADCs are also required to have resolutions in excess of 12 bits and signal bandwidths from 1MHz to 100MHz. The pipelined ADC architecture lends itself well to this kind of applications.

The traditional approach in switched capacitor ADC designs is to employ class A single-stage or multi-stage amplifiers to generate and gain up the inter-stage residue [2]. Whilst such approaches are generally suitable, they quickly become power hungry and inefficient when driving large capacitors. Large sampling capacitors are necessary in order to diminish the thermal noise floor with respect to quantization noise for high-resolution designs. In this paper, we design a class A/B residue amplifier using the industry's first complementary bipolar SiGe process (BiCom3) [3] to mitigate the problem. This technology process features 5V NPN and PNP with $f_t = 20$GHz, precision resistors, capacitors, 5V 0.5µM CMOS, triple-layer metal system, low base resistance and fully dielectric isolation (DI).

II. THE PIPELINED ARCHITECTURE

Pipelining is a method of speeding up manufacturing systems that produce a high volume of products and signal processing systems that process a high volume of samples. When pipelining is applied to a task, it is divided into a number of steps, each requiring an approximately equal amount of time to perform. Figure 1 shows the general form of a pipeline converter, which is a good example of a pipelined signal processor. During each step of the conversion, a certain number of bits of the digital output are resolved. The most significant bits are resolved first; a residue (or remainder) is generated and passed down to the succeeding stages. Therefore each stage is responsible for resolving some segment of the digital output word. The primary advantage of the pipeline architecture [4] is that the inherent concurrence of operations results in a converter
with a conversion rate that is limited only by the time it takes to process the analog information in one stage. In general, each pipeline stage implements a sample-and-hold operation, an A/D conversion, a D/A conversion, a subtraction, and amplification. Because the major factors limiting the speed of this topology are the input sampling and the residue generation and amplification steps, only 2 clock cycles are generally required for each A/D conversion - one for the sampling operation and another for the A/D conversion, D/A conversion, subtraction, and amplification. In principle, the throughput rate of a pipelined converter can approach that of a flash converter incorporating a front-end Sample and Hold.

III. ADC DESIGN

The prototype ADC implemented in this work includes a front-end Sample and Hold (S/H) stage followed by six similar pipelined conversion stages that each resolve 3 bits except for the last 4 bit flash sub-ADC. The inter-stage gain is nominally 4. One bit of redundancy is used in each stage to facilitate digital error correction of stage sub-ADCs (flash comparator) errors [5]. Figure 2 shows a block diagram of most of the ADC. The complete circuit also includes a clock buffer, voltage reference and master bias current generator. The choice of the number of bits resolved by each stage is a trade-off between power, component matching, SNR target and area.

The front end S/H is a ‘flip-around’ bottom plate sampling type [6] as shown in Figure 3. It is designed to acquire a wideband input signal, drive the load of the first stage and relax the design requirements of the first-stage sub-ADC and residue stage by producing a sampled and held signal. It acquires the input on the capacitors during the track phase (P1), and flips the same capacitors to the output during the hold phase. The switches $S_{1A}$ and $S_{1B}$ are implemented with bootstrapped NMOS switches in order to improve their linearity [7] and thus reduce the harmonic distortion. All the other switches are implemented with CMOS transmission gates. The precision capacitors are integrated in trinitride-oxide-poly.

A schematic of the fully differential 3-bit residue stage is shown in Figure 4. It has a nominal gain of 4. It operates on two phases, a sampling phase and a hold phase. During the sampling phase, the input signal is sampled on the eight capacitors. During the hold phase the capacitors are differentially switched to the reference voltages or shorted together. The reference voltage is chosen in the conventional manner based on the digital output of the stage sub-ADC codes in order to generate a residue. This residue is then gained up and passed on to the next stage of the pipeline converter. This process is repeated until all the bits are resolved. The accuracy requirements of each stage are relaxed by the amount of interstage gain preceding it.

The design approach adopted is based on obtaining a high SNR and sampling rate. The SNR for a pipelined ADC referenced to unity full-scale signal range can be approximated as [8],

$$\text{SNR} = 20\log[(2\pi f \Delta f)^2 + \left(1 + e/2\right)^2 + (2^{2N}V_{\text{noise}}/2^N)^2]^{1/2} \quad (1)$$
where, \( f_a \) is the analog input frequency, \( t_s \) is the rms aperture uncertainty, \( e \) is rms DNL of converter and \( V_{\text{noise}} \) is converter electronic noise.

Consider the total input referred thermal noise in the ADC [9],

\[
d_{\text{Thermal}}^2 = d_{\text{Thermal}}^2 + \frac{d_i^2}{G_i^2} + \frac{d_i^2}{(G_iC_d)^2} + \cdots + \frac{d_i^2}{(G_iC_d \cdots C_n)^2}
\]

where \( d_i \) is the RMS thermal noise and \( G_i \) is the inter-stage gain of the \( i \)-th stage respectively. The Sample-and-Hold (S/H) contribution is indicated by the subscript in (2). Total electronic noise is the orthogonal summation of the KT/C noise and amplifier noise assuming they are uncorrelated. For a fully differential implementation [9],

\[
d^2_{\text{elec}} = \frac{1}{2} \frac{2kT}{G^2} \frac{1}{f^2} + V_{\text{opamp}}^2
\]

where \( C_T \) is the total capacitance in the sampling phase and \( f \) is the feedback factor. \( V_{\text{opamp}} \) will depend on amplifier type (e.g., single-stage, multi-stage, etc), technology and design trade-offs. For bipolar devices, the base resistance \( R_b \) must be kept low to reduce amplifier thermal noise.

Equations (2) and (3) are used to extract a value of \( C_T \) which meets a desired noise target. The above procedure was used to determine the 10pF sampling capacitors for this design in order to diminish the KT/C thermal noise floor to less than -80dB with a full-scale input voltage of 4Vpp.

IV. AMPLIFIER DESIGN

To first order, the amplifier output slewing can be derived as,

\[
\text{SR} = \frac{1}{C_L} \frac{V_{FS}}{T_{\text{phase}}} \frac{1}{(\ln(2))}
\]

where in (4), \( 1 \) is the current, \( C_L = 10pF \), \( V_{FS} = 4V \), \( r = 14 \) bits, \( T = 6.25nS \) is the time allocated for slewing, in this case assumed to be 25% of a single clock phase at 20MSPS. Because a fraction of the phase used for generating the residue is spent in slewing; the remaining portion should ensure a settling better than \( V_{FS}/[2^{10.5M}] \), where \( N \) is the resolution of the converter, and \( M \) is the number of bits of the first pipeline stage. A large value of \( M \) relaxes the settling requirements; however, the diminished feedback factor demands larger bandwidths. The use of bipolar transistors is beneficial for two reasons: \( \Delta V \), which is the portion of the transition spent in exponential settling after slewing has occurred, is smaller than in the CMOS counterpart and the larger transconductance provides wider bandwidths.

To obtain high slew rate without consuming excessive small signal bias current and hence power, the approach adopted was to design an input-to-output class AB amplifier as shown in Figure 5 in general form. The main amplifier is buffered by source followers to obtain high input impedance. BJT devices M1 and M2 operate in class A/B mode [\( L = L_{\text{exp}}(V_{be}/N) \)] without tail current limitation. Transistors M3 and M4 are not controlled by the input signal; to avoid additional poles they are biased with a replica fixed voltage \( V_{\text{bias}} \) generated elsewhere (not shown). The push-pull cross-coupled input pairs deliver drive current to the cascoded output legs through current mirrors. Care is taken to properly size the bipolar devices in order to avoid saturation during high slewing current. Simulations show typical DC gain of 100dB, 1GHz bandwidth and 75° phase margin with 10pF load. The slew rate of the circuit is very high because of the class AB operation. Because the amplifier is fully differential, output common-mode control needs to be set to the desired level, 2.5 V in this case. This is implemented using the well-known switched capacitor approach. The common mode feedback signal is connected to devices M23 and M24. Care is taken to ensure the feedback loop is stable.

V. EXPERIMENTAL RESULTS

In the test setup, the sinusoidal input to the prototype ADC is synchronized to the clock signal input. Both signals are coupled through RF transformers. The transformers convert the signals from single ended to fully differential. A center tap also provides a means to set the desired common mode level. Figure 6, Figure 7 and Figure 8 show typical Integral-Non-Linearity (INL) of +/-2LSB, Differential-Non-Linearity (DNL) of +/-0.4 and power spectrum with a 3MHz input respectively at 20MSPS. No dithering or calibration is applied to the converter. Code density test [10] method was used to determine the linearity. Figure 9 shows the chip micrograph in its entirety.

<table>
<thead>
<tr>
<th>Table 1 Performance summary</th>
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<tbody>
<tr>
<td>Resolution</td>
<td>14 bits</td>
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<tr>
<td>Sampling rate</td>
<td>20MSPS</td>
</tr>
<tr>
<td>INL/DNL</td>
<td>+/-2.0LSB, +/-0.5LSB</td>
</tr>
<tr>
<td>SNR</td>
<td>73dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>85dB for 2MHz input</td>
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<tr>
<td>Analog Power/supply</td>
<td>390mW/5V</td>
</tr>
<tr>
<td>Input range</td>
<td>4V_{FS}</td>
</tr>
<tr>
<td>Process</td>
<td>0.5uM SOI/DES, SiGe</td>
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<tr>
<td></td>
<td>complementary Bipolar</td>
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Figure 5. High slewing class A/B operational amplifier.

Figure 6. INL of the converter at 20MSPS versus output code.

Figure 7. DNL of the converter at 20MSPS versus output code.

Figure 8. Power spectrum (dB) versus frequency with 3MHz signal.

Figure 9. Die Micrograph (6mm by 4mm actual size).
VI. CONCLUSION

A 14 bit 20MSPS pipelined ADC designed in complementary SiGe bipolar process is summarized. The main feature is a class A/B amplifier designed to drive large sampling capacitors of 10pF without consuming excessive power. It is noted that more power savings can be obtained if the down-stream stages of the converter are scaled [11], which was not performed in this prototype.

VII. REFERENCES


