Data Converters for Communications: Opportunities and Challenges for Architectures and Analog Design

Franco Maloberti¹,²
¹Department of Electrical Engineering University of Texas at Dallas
P.O. Box 830688, Richardson, TX 75083-0688, USA
²Department of Electrical Engineering University of Pavia
Via Ferrata 1, 27100 Pavia, Italy

Abstract: This paper discusses, from an analog designer viewpoint, present and future system architectures and data-converter solutions. The future scenario is, at the same time, source of opportunities and challenges for both system designers and analog IC designers.

KeyWords: Data converters, Communication systems, Analog design.

Introduction

The expanding use and new services sustain the continuous grow of the communication market. Fig. 1 recalls that, in addition to a constant pace of fixed telephony and a fast expansion of the cellular use, the number of Internet connections demands for high-speed data communication and poses new challenges to architecture definition and circuit design for both fixed and mobile telephony.

Fixed telephony will last for a good number of years. However, its evolution will follow a specific path that is slightly different from the one of the mobile cellular counterpart. The fixed telephony will concentrate on services that require an increasing bandwidth. Bit-hungry applications are not suitable for nomadic use. That will be the domain of fixed telephony. ISDN and ADSL enable very high data-rate. It will be surpassed by VDSL. Instead, cellular market will evolve toward micro and picocells with an increasing customer density [1]. Presently the market tries to nourish the 3-G business with video bit-hungry use. Soon 3-G will support a wide range of new services based on sensor networks and on a different and more sophisticated role of the handset.

Communications: Past Present and Future

The analog telephone started using digital in the 1970s when the SLIC and CODEC enabled digital transmission of voice. In the 1980s the 144 kB/s of the ISDN made possible transmission of data and voice. ADSL introduced in the 1990s boosted the data rate to customer to 2 Mb/s and finally the VDSL will permit a wide band as large as 33MB/s.

On the mobile front after an early service in 1946 the 1G appeared on the market in the 1980s [2]. That first generation enabled just voice transmission using analog modulation. In the 1990s the 2G made possible digital modulation using bands around 900 MHz and 1.8-1.9 GHz. The specifications at the system level created some initial difficulties in the circuit
implementations. Namely the tight requests of SFDR with conversion rate in the 40-60MS/s range have been difficult to meet. However, quality of service and wide coverage sustained a subscribers grow.

The offer of new services and their good acceptance encouraged the definition of new standards for 3G. The first commercial 3G service was launched in Japan in 2001 and the global subscribe reaches 5 million. The slow grow of 3G is an actual challenge. For sustain R&D it is necessary to generate a suitable business. Video applications don’t convince enough customers: the situation calls for new paradigms able to drive the future mobile communication.

Architectures and Standards

Modern communication systems [3], [4] use functions like filtering, modulation, demodulation, clock recovery, gain control, and adaptive equalization. All these function can be both achieved in the analog or in the digital domain. The present trend is to place more of the functionality in the digital side. Thus, new communication architectures and their partitioning move the transition from analog to digital closer and closer to the antenna. As a result, complex algorithms and software-defined operations can be attained. However, the position of the transition point between analog and digital has a direct bearing on difficulties in the data converter design.

The differences between mobile communication standards (GSM, IS-136, IS-95, WCDMA, cdma-2000) lead to stringent performance requirements in the 3G/2G base-station and handset architectures. The evolution of existing 2G architectures towards 3G and beyond requires ensuring backward compatibility. Base-station transceiver must deal with narrowband for 2G (TDMA up to 200 kHz) and wideband CDMA 3G (up to 5 MHz). The adjacent channel blocking features must comply with the most demanding request (100 dB SFDR with GSM). Designing handset faces similar technical challenges, especially for future evolutions that foresee Bluetooth and ad-hoc short-range links with sensor networks. All this problems address a number of design issues involving wideband RF components, wideband ADCs, and high-performance signal processors.

Data converters are key elements in defining the right architecture capable to attain cost effectiveness, multi-standard capability, backward compatibility, and low power consumption. For this, the system designer must know in good details features, limits and future trends in the data converter area. Conversely, analog designers must be aware of problems, requirements and future evolution of standards and architectures used in communication systems [5].

Technologies, Testing and Calibration

The interconnection of smaller and smaller components implements an entire communication system. The evolution of existing architectures towards SoC will embed non-volatile memories. Thus, analog designers will loose, on one hand, some accuracy and linearity but, on the other hand, new devices will become available; digital processing capability and memory will be usable for digital assisted analog design.

High-performance data converters benefit now of special technological steps to have linear adjustable passive elements. Power CMOS is a specialized technology for high-voltage and large currents. In the near future analog, digital and power will merge to provide general-purpose design capabilities, The merging will sacrifice all the features requiring extra masks. The next step will embed non-volatile memories. Thus, analog designers will loose, on one hand, some accuracy and linearity but, on the other hand, new devices will become available; digital processing capability and memory will be usable for digital assisted analog design.

The SoC technology will also change testing of analog interfaces and data converters. Reconfigurable architectures, digital assisted self-calibration and self-test techniques will enhance performances and will facilitate testing.

Data Converter Design Issues

The different standards of communication systems determine challenging data converter specifications. The resolution is often bigger than 12-bit. The linearity must match the SFDR requirements that can exceed 100dB. Finally the signal bandwidth is many ten of MHz. Table 1 summarizes key design issues.

Achieving performances is not just a matter of design expertise but also influences the power consumption.

Table 1

<table>
<thead>
<tr>
<th>Resolution</th>
<th>SFDR</th>
<th>Signal Band</th>
</tr>
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<tbody>
<tr>
<td>12-14 bit</td>
<td>100-105 dB</td>
<td>60 MHz</td>
</tr>
<tr>
<td>• Very low noise</td>
<td>• Linear passive</td>
<td>• Bandwidth</td>
</tr>
<tr>
<td>• Very low spur</td>
<td>• Clock feed-through</td>
<td>• Slew-rate</td>
</tr>
</tbody>
</table>
Increasing resolution and signal bandwidth lead to a practical limit that was not much evident before: above a given resolution and signal band the sampling operation dominates power consumption. To verify this recall that the minimum sampling capacitance \( C_s \) is determined by the \( kT/C \) noise. 1 pF causes 64.5 \( \mu \)V noise spread over the entire Nyquist range. Since the power of a \( V_{pp} \) sine wave is \( 0.125V^2 \) the maximum achievable SNR is 74.8 \( dB \). With oversampling the capacitance value must be diminished by the oversampling ratio (OSR).

Assume that \( R_{eq} \) is the output resistance of the buffer used to charge \( C_s \). The time \( 1/2\pi B \) (\( B \) band of the signal) must be large for ensuring an accurate charging of \( C_s \); say \( \beta \) times \( R_{eq}C_s \). Assume also that achieving \( R_{eq} \) requires a current \( I_{bias}=\alpha V_{DD}/R_{eq} \) drained from \( V_{DD} \). Summing up, the power needed by the buffer is

\[
P_N = \frac{V_{DD}^2}{R_{eq}} = \frac{V_{DD}^2}{V_{pp}} 16\pi kT Q_b \beta \cdot 10^{60_{\text{SNR}}/10}
\]

showing a linear increase with signal band and a \( 4\beta \) increase per each additional bit. Using \( \alpha=2, \beta=8, V_{DD}/V_{pp}=2 \), and \( B=10^3\)Hz we have \( P_{12}=2.6\cdot10^{-2}W \); \( P_{14}=4.2\cdot10^{-4}W \) and \( P_{16}=6.6W(!) \) [7].

Another important design issue is the jitter on sampling clock. The jitter noise power increases with the peak amplitude (\( A \)) and with the frequency of the input sine wave: \( P_j=\alpha^2/\beta<\delta_j^2> \). Thus, \( \alpha=0.5V \) and \( f=100\)MHz need 0.2ps jitter to limit the white noise below 64.5 \( \mu \)V noise (\( SNR=75 \)dB). The result is that an SNR in the 80-90dB range and high bandwidth (> 100 MHz) require clock jitter accuracy that can be achieved with an increasing difficulty.

The above points show that even if we are far from fundamental limits, practical limits hamper the improvement of resolution and bandwidth. The process gain is a parameter typically used by system architects. In the future it will be shared with the data converter designer. The number of bits at the output of an ADC will not be a relevant figure but, instead, the noise corrupting the band of the signal.

Distortion is another key design issue. It is due to static and dynamic effects. Assume that a non-linear transformation represents it

\[
y = \alpha + \beta x + \gamma x^2 + \delta x^3
\]

with an input sine wave \( x=\sin(\omega t) \) the output is

\[
y = \alpha + \beta \sin(\omega t) + \frac{\gamma}{2} A^2 [1 - 2 \cos(2\omega t)] + \\
+ \frac{\delta}{4} A^3 [-\sin(3\omega t) + 3\sin(\omega t)]
\]

with \( A=0.5 \) a -100dB third order harmonic requires \( \delta<3.2\cdot10^{-4} \). Having passive components with voltage coefficients better than few \( ppm \) is still possible. Designing op-amps or OTAs with 100dB of DC gain is difficult but attainable. However, exceeding those figures, especially when technology must accommo-

date analog, digital and power needs is unlike.

The few elements discussed in this section show that the performances of state-of-the-art data converters become being constrained by practical limits. Again, the definition of new communication standards and the design of new architectures require a close cooperation with analog and digital circuit designers.

### Data Converter Architectures

Pipeline is a popular architecture for high-speed high-resolution Nyquist-rate ADC. A typical block diagram is shown in Fig. 4 [8]. The number of bit per cell and the number of cells are design variables.

![Architecture of a pipeline ADC.](image)

The required accuracy decreases along the pipeline. As a result, critical parts of the design are the input T&Hs and the first cell (assuming \( b_1>3 \)) of the pipeline. An SFDR as high as 100dB requires using very linear passive components, bipolar technologies and special care in the T&H design. The required speed and linearity rely on the \( g_o \) of bipolar transistors and also call for complementary vertical BJTs. The use of sub-micron CMOS obtains very high speed but the linearity is such that the SFDR remains in the 85dB range. Moreover, power consumption ranges between 0.7 and 2\( W \). It is more than 8\( W \) for 400 MS/s.

A study of literature and an exam of existing products determine the estimation of the performances time evolution (assuming a power consumption below 2\( W \)) shown in Fig. 5. The SFDR for BJT and CMOS technologies will not improve significantly.

![Pipeline ADC feature evolution.](image)
The CMOS will catch the BJT speed in a few years. Power consumption of commercial realizations is relatively high and makes high-performance pipeline architectures suitable only for 2G base-stations.

The trends of Fig. 5 motivated research on alternative data converter architectures. They are mainly based on sigma-delta. The sigma-delta method uses oversampling and noise shaping for limiting the quantization noise in the signal band. Key parameters of sigma-deltas are the order $L$ and the number of bits $M$ of the oversampled quantizer. The oversampling ratio $OSR$ is defined as $f_s/(2B)$. The $SNR$ is given by

$$SNR = 6.02 \left[(M-1) + (L + 0.5) \cdot OSR \right] - 10 \cdot \log \left( \pi \frac{1}{2} \right)$

Even using sigma-delta does not enable wide-band and low-power: the gain bandwidth $f_d$ of the op-amp must be at least $4 \cdot B \cdot OSR$. If the $SNR$ target with $V_i=1V$ is $85dB$ a $75MHz$ wide-band conversion and $M=1$ require a fourth order modulator with $OSR=17$. It turns out that $f_s=5.1GHz$ and $C_w=1.17pF$. The value of the average current $V_iC_wf_d$ is $12mA$. A multi-bit solution relaxes a bit the requirements: a third order, $M=5$ architecture decreases the oversampling by more than 2x while the sampling capacitor slight increases. However, the power consumption is still too high for low-power applications.

Small-band pass-architectures better exploit noise shaping. The major limit of band-pass architectures comes from mirror images that fall in the signal band. The use of special architectures based on the n-path technique moves the mirror images far away from the signal band [9] and can potentially obtain $85dB$ SFDR with $5MHz$ signal-band ($IF-40-80MHz$) and power consumption lower than $0.1W$.

The data converters used in ADSL require $SNR$ better than $90dB$ (in the echo canceller). That figure is challenging but achievable since the conversion rate is not particularly high ($4.4Ms/s$). The main concern in ADSL is about low cost. Therefore, the architectures require minimum chip area. Solutions that meet the ADSL requirements are the pipeline and 4-th order Mash Sigma-delta or second order multi-bit sigma delta. The sampling frequency used is some ten of $MHz$ [10].

The 3G standards enable using data converters in the handset. In addition, peripherals that use Bluetooth need data converter. Depending on the architecture the required $SNR$ is around $60dB$ for the WCDMA and $72dB$ for Bluetooth. The signal band is $1.9MHz$ for WCDMA and $1MHz$ for Bluetooth. This kind of requirements is met with sigma-delta with a small oversampling. The clock frequency is $39.4MHz$ leading to $OSR=10$ for WCDMA and $OSR=19$ for Bluetooth. The key requirement is to dissipate minimum power. With $OSR=10$ it is necessary to use a 2-bit $2+1$ Mash sigma-delta or a 4-bit second-orders sigma-delta. The state-of-the-art in terms of power

\[
\text{FoM} = \frac{P}{2^M f_s}.
\]

Fig. 6 – $\Sigma \Delta$ power consumption; GSM and WCDMA.

The figure of merit measures power effectiveness

For oversampled data converter we have to use $2B$ instead of $f_s$. Therefore, the figure of merit of the implementation in [11] is $2.5pJ/Conv$-level. State-of-the-art values are well below that figure. It is expected that in few years, as shown in Fig. 6, the power consumption will go down to $0.5mW$. The new architectures will exploit minimum sensitivity to finite gain and bandwidth of the op-amp, and will use double sampling or op-amp sharing.

**Conclusions**

The progress of data converters performances is a unique opportunity for defining new communication systems with an increasing use of signal processing. However, a number of practical limits (namely power consumption and linearity) make uncertain the data converter progress. Thus, defining the new standards and designing architectures requires a good knowledge of opportunities and challenges that the analog designer faces.

**References**


