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9.2 A Low-Power Multi-Bit $\Delta \Sigma$ Modulator in 90nm Digital CMOS without DEM

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There is an increasing demand for low-power, high-signal-bandwidth SoCs. The challenges faced by delta-sigma ($\Delta \Sigma$) modulators used in these applications are two folds: they must provide large dynamic range and they must coexist with the digital core in a digital CMOS process.

This second-order multi-bit delta-sigma modulator ($\Delta \Sigma M$) uses a 4b ADC. The truncation of the digital ADC output, the shaping of the error, and its cancellation, enable using a 3-level DAC in the main feedback loop and a 5-level DAC in the second integrator feedback loop. This design uses $f_{\text{clk}}=40$MHz. The circuit achieves 51dB SNDR with OSR=10 and 72dB SNDR with OSR=50. Accordingly, the architecture meets the requirements of many applications including wireless base-band systems [1], [2].

The use of a second-order modulator reduces the digital filter complexity. Moreover, a second-order loop is good for low power. A third-order modulator [3], possibly achieved with a MASH architecture that increases the number of bits in the digital filter, requires an additional opamp that is an important source of power consumption. For low OSR, the same SNR is obtained with a multi-bit quantizer that is not particularly hungry. On the other hand, the problem of mismatch between unity elements used in the feedback DACs would need to be resolved. The dynamic element matching (DEM) technique is often used to transform mismatch into noise; but, with a low OSR and DAC resolution $>5$b, it is difficult to effectively utilize DEM. Having many unit elements to average causes tones in the signal band for low input signals. Moreover, the total capacitance would be relatively large even if the unit capacitance is minimum.

As mentioned above this circuit avoids using DEM by employing a truncation error shaping and cancellation method [4]. Figure 9.2.1 illustrates the truncation and error shaping technique. The output $Y$ of the second-order $\Delta \Sigma M$ is a multi-bit digital signal. It is passed through two digital $\Delta \Sigma M$s with order $A$ and $B$ respectively. The number of bits at the outputs $Y_1$ and $Y_2$ are reduced. $Y_1$ and $Y_2$ are the superposition of $Y$ (no delay) and a given shaping of the truncation noise terms $e_1$ and $e_2$. By inspection of the circuits we find

$$Y = X \cdot z^{-2} + \varepsilon (1- z^{-1})^2 - e_1 z^{-2} (1- z^{-1})^4 - 2 e_2 z^{-4} (1- z^{-1})^6 + \delta_1 $$

The contributions of $e_1$ and $e_2$ become negligible with respect to $\varepsilon$ if $A=3$ and $B=2$. Obtaining no delay in the digital $\Delta \Sigma M$ is possible since the flash ADC can lend some time to the digital processor. The circuit as implemented minimizes the complexity and uses a lower order in the digital $\Delta \Sigma M$ ($A=2$ and $B=1$) by taking advantage of the second method used; the error cancellation technique. The approach is described with the help of Fig. 9.2.2. The quantization error $e_1$ is multiplied by 0.5$z^{-1}(1-z^{-1})$ and added to the input of Dig-$\Delta \Sigma$e. The output of Dig-$\Delta \Sigma$e equals the noise shaped term $e_1(1- z^{-1})^4$ passed through the analog block 0.5$z^{-1}(1-z^{-1})$. Thus, the two contributions are cancelled out. A similar cancellation is achieved for $e_2$. A possible mismatch between the analog and digital transfer functions produces some residual, but that effect is likely negligible thanks to the second-order noise shaping. The system transfer function is

$$Y = X \cdot z^{-2} + \varepsilon (1- z^{-1})^2 - e_1 z^{-2} (1- z^{-1})^4 - 2 e_2 z^{-4} (1- z^{-1})^6 + \delta_1 $$

$\delta_1$ and $\delta_2$ are the mismatches between the analog and digital cancellation paths and are, ideally, zero. $e_1$ and $e_2$ are bigger than $\varepsilon$ by 2$^2$ and 2$^4$ ($P$ and $Q$ are the number of truncated bits in the Dig-$\Delta \Sigma$ and Dig-$\Delta \Sigma$e blocks). If $\delta_1$ and $\delta_2$ are on the order of 1%, they enable a truncation up to 4 bits without affecting the SNDR.

The architecture of Fig. 9.2.2 achieves low power. It requires using only two opamps, 15 comparators and some digital logic. The reference voltage of the $\Delta \Sigma M$ is ±800mV$_{pp}$ fully differential. System-level simulations show that with single-sampling an opamp gain larger than 60dB and unity-gain bandwidth larger than 80MHz are required. The OTA used for the integrators is a 2-stage amplifier; the small output resistance of the sub-micron transistors requires using a folded cascode in the first stage. Miller compensation yields a bandwidth of 100MHz with an open-loop gain of 70dB. The total current drawn is about 0.65mA for the first-stage integrator and 0.4mA for the second stage.

The two DACs use 3 levels (–1, 0, +1) and 5 levels (–1, –0.5, 0, 0.5, 1) respectively. Figure 9.2.3 shows the implementation with switched capacitors. The sampling capacitor $C_1$ is chosen to be 100fF, and $C_2$ is 200fF. 15 comparators made with differential pre-amplifiers and latches are used in the 4b flash ADC. The current consumption of the 15 comparators is 0.3mA. A poly resistor string made by 32 equal 250$\Omega$ resistors divides an external reference to produce the reference voltages. The digital $\Delta \Sigma M$ processing functions were coded in VHDL, simulated with Modelsim and synthesized in Synopsys. The dynamic current consumption of the digital processor is 0.1mA. The prototype is fabricated in a standard 90nm digital CMOS process. The total area of the modulator including the digital circuits is 0.4mm$^2$ and draws 1.6mA at 1.3V including dynamic contributions, which is within the range supported by the process. A TQFP 64 pin package is used. Figure 9.2.7 shows the chip microphotograph. The measured performance agrees well with the transistor-level simulations. Figure 9.2.4 shows the 65536-point FFT plot of the output data. The input sine wave is ~6dBFS at 533.3kHz. The noise floor below ~100dBc is, as expected, mainly due to $kT/C$ noise. The gains and bandwidths of the OTAs do not degrade performance. The SNDR is 51dB with OSR=10 ($B_m=2$MHz). Similar measurements for OSR=20 and OSR=50 show SNDR equal to 61dB and 72dB respectively. Figure 9.2.5 shows the SNR versus amplitude plots for the three cases. The 0dB crossings (DR) are at ~78dB, ~66dB and ~58dB respectively, as shown in Fig. 9.2.5. Figure 9.2.6 summarizes the results.

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References:

Figure 9.2.1: Truncation Error Shaping of Second-Order ΔΣM.

A, B, C, and 1, 2, 3, 4 are synchronous with \( \phi_i \).

Figure 9.2.2: Truncation Error Cancellation of Second-Order ΔΣM.

Figure 9.2.3: First and Second Integrator.

Figure 9.2.4: 65536-point FFT of Output (OSR=10).

Figure 9.2.5: SNDR Curve for Different OSRs.

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<th>OSR</th>
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<tr>
<td>Dynamic Range</td>
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Figure 9.2.7: Die Photograph.