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Heap Charge Pump Optimisation by a Tapered Architecture

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Abstract - The heap charge pump represents an attractive voltage multiplier scheme in integrated circuits where only low-voltage devices are available. This paper presents a performance optimisation of the heap charge pump achieved by using a tapered architecture. The proposed optimisation allows improvements on the order of 30% in terms of maximum output voltage as compared to the conventional heap charge pump. A mathematical description of both the conventional and the proposed structure was developed. MATLAB[®]-based simulation results demonstrate the effectiveness of the proposed scheme.

I. INTRODUCTION

The evolution of microelectronic technology allowed a dramatic scaling down of all parameters in integrated circuits. In particular, the request for low power dissipation and minimum area occupation in electronic devices pushed the use of low supply voltages and small component sizes. However, a number of applications exists where the reduction of operating voltages is not possible because of intrinsic physical limits.

In particular, the operations of flash memories require the availability of high voltages [1]. In modern devices, such high voltages must be produced on-chip by using the standard supply voltage V_{dd} . To this end, integrated high-voltage generators, which are generally referred to as voltage multipliers and are typically based on the charge pump approach, are used. The goal is to charge a load capacitor connected to the output node of the voltage multiplier so as to obtain an output voltage higher than V_{dd} .

In flash memories, during program operations, the gates of cells belonging the addressed word-line have to be driven to ~ 10 V. The capacitive load C_L associated to the final stages of the row decoder and the selected word-line is rather high. For instance, in 0.18- μm technology, the capacitive load in the case of a 4-Mb sector is about 200 pF.

The most popular voltage multiplier topology in Flash memories is Dickson charge pump [2]. However, all Dickson-derived schemes [3], [4] suffer from a number of drawbacks. The main limit consists in large area occupation when a high number of stages in low-voltage fabrication processes is required. Indeed, in a number of low-voltage processes, poly1-to-poly2 capacitors are not available and, hence, capacitors are realized by using the gate capacitance of MOS transistors. Pump capacitors that have to sustain a high voltage must thereby be realized by using the series of two or more capacitors ("capacitor split" approach), in order to prevent oxide breakdown. The higher the number of stages, the higher the number of pump capacitors to be split, which dramatically increases silicon area occupation.

Figure 1 – Ideal heap charge pump
(switch configuration corresponds to the set-up phase).

The heap pump [5] represents a different approach to realize a voltage multiplier. This circuit, schematically depicted in Fig. 1, is based on the cascade of N identical stages, each containing a capacitor C_i ($1 \leq i \leq N$) and two switches S_A and S_B . In the conventional topology, all capacitors are equal ($C_i = C$). The operating principle of

the heap pump is different as compared to the Dickson scheme. The basic idea consists of charging the N capacitors C_i between V_{dd} and ground, in a phase referred to as set-up (switches S_A closed, switches S_B closed to ground, and switch S_C open), and then connecting them in series, during a phase referred to as pump-up (switches S_A open, switches S_B closed between two adjacent capacitors, and switch S_C closed). The charge stored in the series connection is shared with the load capacitor C_L and, therefore, a high output voltage is obtained in the steady state. A clock signal controls the two working phases. It should be pointed out that the same scheme can be used to realize a negative high voltage generator, by only modifying the series connection of capacitors C_i [5]. It is worth to underline that the voltage across each capacitor of the charge pump (except C_L) is relatively low (i.e., not larger than V_{dd}) in any operating phase. Therefore, capacitors can be realized by means of a single MOS transistor, without resorting to the capacitor split approach as in the case of Dickson charge pump. This way, silicon area occupation can be kept sufficiently low. However, this scheme presents a great drawback. Its operation is dramatically affected by the presence of the stray capacitances associated to the top and the bottom plate of each capacitor C_i , which reduces the maximum achievable output voltage, as will be shown in the Sections II and III.

In this paper, a tapered architecture that improves heap charge pump performance in terms of output voltage is presented. A qualitative and a mathematical description of both the conventional and the proposed heap charge pump are provided. MATLAB[®]-based simulation results are given to demonstrate the effectiveness of the proposed scheme.

II. CONVENTIONAL HEAP PUMP

During the pump-up phase, capacitors C_i in Fig. 1 are connected in series, thus transferring a given amount of charge to the load capacitor C_L . Let us assume that, during the pump-up phase, a charge $+q_{out}$ is transferred from the upper plate of capacitor C_N to the upper plate of C_L . A charge $-q_{out}$ must therefore leave the lower plate of C_N . As a consequence, capacitor C_N is discharged by a charge amount equal to q_{out} . The charge $-q_{out}$ flows through the only conductive path available and reaches the upper plate of capacitor C_{N-1} , thus neutralizing a part of the positive charge stored in this element. A charge $-q_{out}$ is therefore transferred from the lower plate of C_{N-1} to the upper plate of capacitor C_{N-2} , thereby discharging C_{N-1} . The same considerations hold for all other capacitors in the pump. It is apparent that the voltage across any capacitor C_i is reduced by an amount $V_L = q_{out}/C$ with respect to the initial value V_{dd} .

Fig. 2 shows a heap charge pump scheme also including stray capacitors. Here and in the following, the

stray capacitor associated to the top and the bottom plate of capacitor C_i will be referred to as C_{ti} and C_{bi} , respectively. Capacitor C_{ti} is charged to the supply voltage V_{dd} during the set-up phase, and to a higher voltage during the pump-up phase. Capacitor C_{bi} is discharged to ground during the set-up phase, while its behaviour is the same as for $C_{t(i-1)}$ ($1 < i \leq N$) during the pump-up phase. During the pump-up phase, each stray capacitor can be assimilated to a (small) capacitive load, whose behaviour is the same as described above for capacitor C_L . During this phase, any capacitor C_i must therefore provide the charge drawn by the stray capacitors belonging to stages $i, i+1, \dots$, and N . This reduces the voltage across any capacitor C_i and, hence, the maximum voltage achievable at the output node. As a consequence, the charge loss (and, hence, the voltage) in capacitors C_i belonging to the first stages of the charge pump is higher than the charge loss of the capacitors belonging the last stages.

Figure 2 – Circuit diagram of a heap charge pump including stray capacitors.

III. PERFORMANCE ANALYSIS

We will now analyze the behaviour of the heap pump during the pump-up phase, assuming, as an initial condition in this phase, that the voltage across capacitors C_i and C_{ti} is equal to V_{dd} , and the voltage across capacitors C_{bi} is zero. The voltage on the upper plate of capacitor C_i will be referred to as V_i .

To evaluate the performance loss due to stray capacitors, we must find an expression for voltage V_i at the i -th node of the heap pump as a function of time. In particular, it is our interest to find an expression for the maximum achievable output voltage. The charge balance at the j -th clock cycle at the node referred to as 1 in Fig. 3, which depicts a detail of the pump, yields:

$$(C_{t1} + C_1)V_{dd} - C_2V_{dd} = (C_{t1} + C_1 + C_{b2})V_1(j) - C_2(V_2(j) - V_1(j)) \quad (1a)$$

where $V_i(j)$ represents voltage V_i at the considered j -th clock cycle. The left term in (1a) represents the charge (positive and negative, respectively) stored in the upper plates of C_1 and C_{i1} and in the lower plate of C_2 at the beginning of the pump-up phase. The right term represents the charge present in the above plates and in the upper plate of C_{b2} at the end of the pump-up phase, when charge transfer is over. The following equations hold for the i -th and the N -th stage, respectively:

$$(C_{ti} + C_i)V_{dd} - C_{i+1}V_{dd} = (C_{ti} + C_{b(i+1)})V_i(j) + C_i(V_i(j) - V_{i-1}(j)) - C_{i+1}(V_{i+1}(j) - V_i(j)) \quad (1b)$$

$$(C_{tN} + C_N)V_{dd} + C_L V_N(j-1) = (C_{tN} + C_L)V_N(j) + C_N(V_N(j) - V_{N-1}(j)) \quad (1c)$$

Equations (1a), (1b), and (1c) are a set of N equations, where the N variables are the open-circuit voltages $V_1, V_2, \dots, V_N$ at each node of the pump.

In the conventional heap pump in Fig. 2, we assume $C_{t1} = C_{t2} = \dots = C_{tN} = C_t$, $C_{b1} = C_{b2} = \dots = C_{bN} = C_b$. The maximum output voltage V_N , i.e., the value reached by voltage V_N at the end of the set-up transient, can be obtained by solving the above equation set iteratively (for $j = 1, 2, \dots$).

Figure 3 – Detail of a heap charge pump (first two stages) during the pump-up phase.

Fig. 4 represents the calculated (MATLAB®) steady-state open-circuit output voltage normalized to V_{dd} obtainable by an N -stage heap pump ($N = 1$ to 11), as a function of stray capacitor sizes (C_t/C and C_b/C ranging from 1% to 10%). The decrease in the output voltage (whose ideal value is $(N + 1)V_{dd}$) for increasing values of C_t/C and C_b/C is apparent. Furthermore, it can be seen that when the sizes of the stray capacitors increase, there is substantially no benefit in adding many stages to the charge pump: due to the charge loss caused by the additional stray capacitors, the increase in the output voltage is too small to be really advantageous.

The same mathematical approach can also be used to analyze the voltage at each node of the charge pump as a

function of time. Fig. 5 represents the MATLAB® solution of equation set (1a), (1b), and (1c) for an 11-stage heap pump, with a total capacitance $C_{TOT} = 150$ pF ($C = 13.6$ pF), a load capacitor $C_L = 200$ pF, a supply voltage of 1.8 V, and stray capacitors $C_t = 0.01C$ and $C_b = 0.02C$ (that are typical values for a 0.18- μ m technology). Each node of the grid represents the voltage at the i -th node of the pump at the end of the pump-up phase in the j -th clock cycle. The steady-state output voltage turns out to be equal to 10.8 V.

Figure 4 – Open-circuit output voltage of a heap charge pump as a function of stray capacitors sizes (C_t/C and C_b/C) and of the number of stages (N) ($V_{dd} = 1.8$ V).

Figure 5 – Voltage at each node in an 11-stage heap charge pump as a function of time ($V_{dd} = 1.8$ V; $C_i = 13.6$ pF, $C_t/C = C_b/C = 0.01$; $C_L = 200$ pF).

IV. TAPERED ARCHITECTURE

In the previous Section, it has been shown that the presence of stray capacitors reduces the open-circuit output voltage achievable by a heap charge pump. In order

to overcome this drawback, we propose a heap charge pump in which capacitors of different stages have different sizes. More specifically, the capacitor in any $(i+1)$ -th stage is smaller than the capacitor in the preceding i -th stage by a constant factor, i.e. $C_{i+1} = C_i w$ ($w < 1$). For this reason, hereinafter, the circuit will be referred to as tapered heap pump. The constant w plays the role of tapering coefficient. The basic idea is to store a larger amount of charge in those capacitors where a larger charge amount is removed during the pump-up phase. Therefore, capacitors $C_1, C_2, \dots$, will be able to provide the charge to all the cascaded stray elements while still suffering from a reduced voltage loss. Assuming $C_1 = C$, the size of the other capacitors turns out to be $C_2 = Cw$, $C_3 = Cw^2$, ..., $C_N = Cw^{N-1}$. The tapered heap pump operation is still described by the set of N equations (1a), (1b), and (1c).

To determine the optimum component sizes for the proposed scheme, the achievable open-circuit output voltage was analyzed as a function of the tapering coefficient value. In this analysis, we considered the same values of total capacitance, load capacitor, supply voltage, and top and bottom plate stray capacitors adopted for the conventional heap pump in the previous Section. The obtained results are shown in Fig. 6. The best output voltage (13.8 V) is obtained with a tapering coefficient equal to 0.75. The maximum output voltage (10.8 V) for the conventional heap pump ($w = 1$) corresponds to the value previously shown in Fig. 5. The maximum gain of a tapered heap pump with respect to the conventional heap pump can therefore be high as 27.8%.

Figure 6 – Maximum output voltage of a 11-stages tapered heap pump as a function of the tapering coefficient w ($V_{dd} = 1.8$ V).

The solution of equation set (1a), (1b), and (1c) for an 11-stage tapered heap pump ($w = 0.75$) is shown in Fig. 7. The behaviour of the voltage at the pump nodes as a function of time is different as compared to the case of the conventional heap pump. In the first clock cycles, the charge transferred from any capacitor of the charge pump

to the load and the stray capacitors is higher than the charge stored in the smaller capacitors of the last stages during the set-up phase. As a consequence, in the first cycles, the highest voltage is not observed at the output node, but at an internal node. As expected, in the steady state, the output voltage reaches 13.8 V.

Figure 7 – Voltage at each node in a tapered heap pump ($w = 0.75$) as a function of time.

V. CONCLUSIONS

In this paper, a tapered architecture for heap charge pumps has been presented. The proposed circuit allows improvements on the order of 30% in terms of achievable maximum output voltage as compared to the conventional heap charge pump. A qualitative and a mathematical description of both the conventional and the proposed structure has been provided. MATLAB[®]-based simulation results demonstrated the effectiveness of the proposed scheme.

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