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Use of non-linear Chua's circuit for on-line offset calibration of ADC

A. Cabrini* and F. Maloberti*

Abstract – The offset of an ADC is one of the main limitations for interleaved architectures. The method proposed here enables a precise measurement of the offset while the ADC operates and introduces a minimum disturb to the output result. The method exploits a random modulation by +1 or -1 of the input signal. The modulating signal is the wide-band output of a Chua circuit passed through a comparator. The resulting spread spectrum can be easily distinguished by the dc offset and reconstructed in the digital domain with a synchronous demodulation. The use of a digital accumulator extracts the offset. The accumulation time can be many clock periods (like 10^6) thus permitting an excellent accuracy in the offset measurement. Simulations of the proposed approach at the behavioral level confirm the effectiveness of the method. It is shown that the offset of a 12-bit ADC can be measured with a 0.1 LSB accuracy.

1 INTRODUCTION

The offset of a single ADC is important only for some specific applications. By contrast, when many ADCs are used in a system, the mismatch between the offset of different ADC is source of important limitations. For example in interleaved architectures with n-paths, the offset mismatch generates a periodic signal at f_{ck}/n . The corresponding tones are in the Nyquist interval and generate spurs affecting the output spectrum. Even the gain mismatch is responsible of errors; however, a possible error in the gain is caused by passive component mismatch and for modern technologies it is possible to ensure accuracies in the 0.1% range or better.

The calibration of the offset can be done off-line or on-line [1], [2], [3]. The off-line solution requires a specific time-slot for the calibration. It can be done at the power-on or when the converter is idle. On-line calibration is preferred. The calibration is done periodically during the normal operation without disturbing the measure of the converter. Therefore, a possible slow drift of the offset is compensated for.

This paper uses the basic idea proposed in [4] but improves the method by employing the non-linear Chua's circuit for generating a signal that is key in obtaining good results. The nonlinear Chua's circuit can be implemented using simple analog circuits and requires limited additional power consumption. The results obtained here show that the measure of the

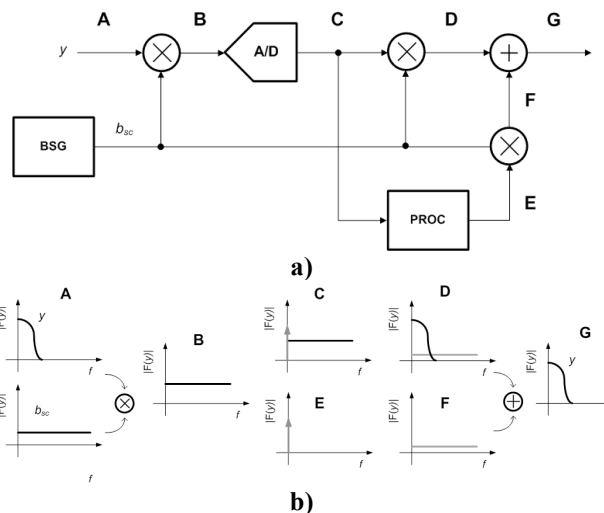


Figure 1: Block diagram of the proposed solution a), equivalent representation in the frequency domain b).

offset with an accuracy better than $2 \cdot 10^{-3}$ is performed using 10^4 clock periods, an order of magnitude less than the result reported in [4].

2 ON-LINE OFFSET CALIBRATION

The basic idea of the used method is to perform a modulation of the input signal by ± 1 (Figure 1). The modulation is straightforward with fully differential circuits. The input terminals to the ADC are switched according to a given modulating control signal. After the conversion the digital output is synchronously modulated again.

The method is a generalization of the chopper stabilization technique. The two synchronous modulations leave unchanged the spectrum of the input signal while the second modulation moves the offset from dc. If the modulation is periodic, for instance at $f_{ck}/2$, the offset goes at $f_{ck}/2$. Having a signal at Nyquist can be problematic because of the effect of a possible non-linear response.

The use of an uncorrelated bit stream of +1 and -1 spreads the spectrum of the input after the first modulation and transform the spectrum of the offset into white noise after the second modulation. Therefore, the effect of offset is transformed into

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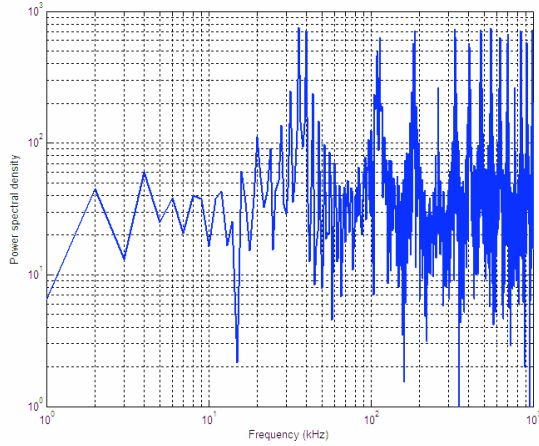


Figure 2: Power spectral density of the output binary stream of a PRSG.

noise. However, the SNR of the converted signal is worsened. The above points are illustrated in Fig. 1. The bottom part shows the spectra in different points of the processing chain. Observe that after the ADC we have a dc term corresponding to the offset. In the same spectrum we also have to account for the quantization noise. It is not visible on the figure since its contribution is negligible with respect to the white spectrum representing the signal.

Observe that the spectrum after the ADC contain the dc term caused by the offset. A low-pass filter with very low bandwidth enables measuring its analog-to-digital conversion. Then, the modulated estimation of the offset is subtracted in the digital domain to obtain an offset-free result.

The effectiveness of the method relies on the modulating signal. The bit-stream generator (BSG) should give at the output a sequence of ± 1 capable to transform any input into a spread spectrum signal. The previous implementation described in [4] used a pseudo random number generator [5] followed by a comparator. Unfortunately any pseudo random sequence is periodical. If the input signal contains a spectral term at the same frequency of the pseudo random sequence the modulation produces a dc term that cannot be distinguished from the offset.

In Figure 1, when the modulation is not considered, the signal at node C can be expressed as:

$$y_C = y + \varepsilon_{dc} \quad (1)$$

where y is the input signal and ε_{dc} is the error introduced by the A/D converter. Nevertheless, by modulating the input signal y by $(2b_{sc} - 1)$ it follows:

$$y_C = (2b_{sc} - 1) \cdot y + \varepsilon_{dc}. \quad (2)$$

By averaging y_C we obtain:

$$\langle y_C \rangle = \langle y \cdot (2b_{sc} - 1) \rangle + \langle \varepsilon_{dc} \rangle. \quad (3)$$

Actually, if the digital sequence b_{sc} is a random sequence of 0 and 1 with a white-noise spectrum (not correlated with the signal) and equal number of 1 and 0, the signal $\langle y \cdot (2b_{sc} - 1) \rangle$ vanish and $\langle y_C \rangle$ become equal to ε_{dc} .

3 BIT-STREAM GENERATOR

As mentioned above, to properly operate, the proposed solution requires a suitable bit-stream generator for the binary sequence b_{sc} used to modulate the digital signal y . In fact, to evaluate the effectiveness of the proposed approach, the autocorrelation of the output signal of the BSG must, if possible, zero outside of a compact set (with the compact set as narrow as possible). This is mandatory in order to reduce the sensitivity of the on-line offset measure to the input signal. A feasible solution can be the use of a digital pseudo-random sequence generator ($PRSG$). Nevertheless, a $PRSG$ has a periodic spectrum (Figure 2). To reduce autocorrelation of the bit-stream the use of a non linear circuit is an appealing solution. In fact, the most attractive feature of non-linear systems is their intrinsic unpredictability (even if the time evolution of the system is completely deterministic) thus allowing an improved white noise generator to be designed. In our case, we decided to use a Chua's circuit.

3.1 Chua's circuit

Figure 3 shows the conceptual scheme of a Chua's circuit. The state equations of the system are given by:

$$\begin{cases} \frac{dV_1}{dt} = \frac{1}{C_1} \cdot \left[\frac{V_2 - V_1}{R} - f(V_1) \right] \\ \frac{dV_2}{dt} = \frac{1}{C_2} \cdot \left[\frac{V_1 - V_2}{R} + i_3 \right] \\ \frac{di_3}{dt} = -\frac{1}{L} \cdot V_2 \end{cases} \quad (4)$$

and the non linear element $f(V_1)$ is:

$$f(V_1) = G_b V_1 + \frac{1}{2} (G_a - G_b) [|V_1 + V_e| - |V_1 - V_e|] \quad (5)$$

where V_e is the break voltage of the non-linear element and G_a and G_b are the slopes of the segments in Figure 3. From (4), the dynamic of the system can be calculated by specifying L , C_1 , C_2 , R , G_a and G_b . As shown in [6], when the behavior of the circuit is the main interest, (4) can be rearranged as follows:

$$\begin{cases} \frac{dx}{d\tau} = \alpha \cdot [y - x - f(x)] \\ \frac{dy}{d\tau} = x - y + z \\ \frac{dz}{d\tau} = -\beta y \end{cases} \quad (6)$$

Where $x \equiv V_1/V_e$, $y \equiv V_2/V_e$, $z \equiv i_3/(R/V_e)$, $\alpha \equiv C_2/C_1$, $\beta \equiv R^2 C_2/L$ and $a \equiv RG_a$, $b \equiv RG_b$. Finally, the variable τ is a dimensionless time and is equal to t/RC_2 . The same, (5) can be expressed as:

$$f(x) = \begin{cases} bx + a - b & \text{if } x \geq 1 \\ ax & \text{if } |x| \leq 1 \\ bx - a + b & \text{if } x \leq -1 \end{cases} \quad (7)$$

The main advantage of such a representation is the possibility of easily adjust the system behavior thus allowing a wide band BSG to be simply realized.

3.2 The BSG

To generate the wide-band digital output sequence b_{sc} , two Chua's circuit were used each one having different operating parameters. This way, their time evolution turn out to be widely uncorrelated. By using a suitable comparator (with the inputs connected to the output of the Chua's circuits), it is possible to generate a wide band digital signal. Furthermore, to guarantee the same number of 0 and 1 in the output sequence, an extra digital modulation can be added.

Figure 4 shows the power spectral density of the BSG binary sequence. In figure, an ideal white Gaussian noise is also represented (gray line). As it can be seen, the spectrum of the generated binary sequence has a wide band and, compared with the power spectrum of a PRSG, has adequately "white" behavior and, most important, does not show tones in the spectrum. This way, the advantages proffered by the proposed method can be fully exploited and effectively evaluated.

4 SIMULATION RESULTS

Behavioral simulations have verified the proposed method. Figure 5 shows the basic block diagram of the calibration network. In this scheme, the error ϵ_{dc} is a constant value (in our case 0.05 % of the dynamic range); after the scrambling controlled by the BSG binary sequence, the measured error $\epsilon_{dc,meas}$ is added to the input signal. The quantization is modeled using an ideal converter. In this ideal case,

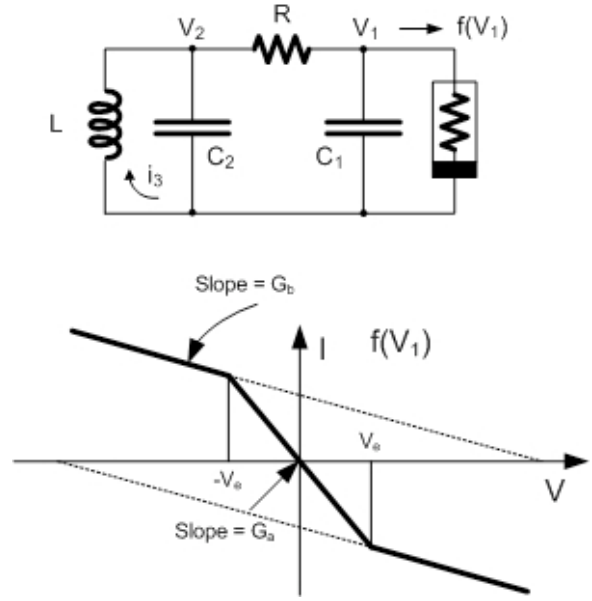


Figure 3: Conceptual scheme of the Chua's circuit.

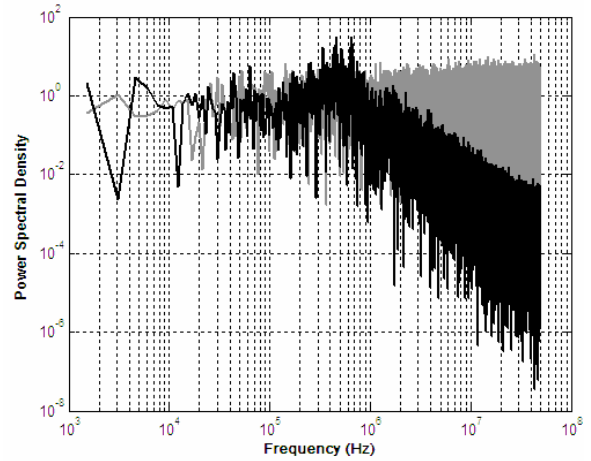


Figure 4: Power spectral density: BSG (black line), ideal numeric white Gaussian noise (gray line).

since the quantizer does not foresee any delay, the same binary sequence b_{sc} can be used to perform all the required modulations. In real case, since the conversion process introduces a delay, a suitable delay element will be used. Finally, the accumulators leads to the measure of the mismatch. In particular, the top one is the integral of the error ϵ_{dc} while the bottom element carries the measured the error $\epsilon_{dc,meas}$. The input signal generator used for simulations is the combination of four generators: a band-limited noise, two sine-wave generators and an offset. Figure 6 shows the corresponding outputs of the two accumulators. The measure of the offset is carried out with an accuracy better than $2 \cdot 10^{-3}$ and can be performed using about 10^4 clock periods.

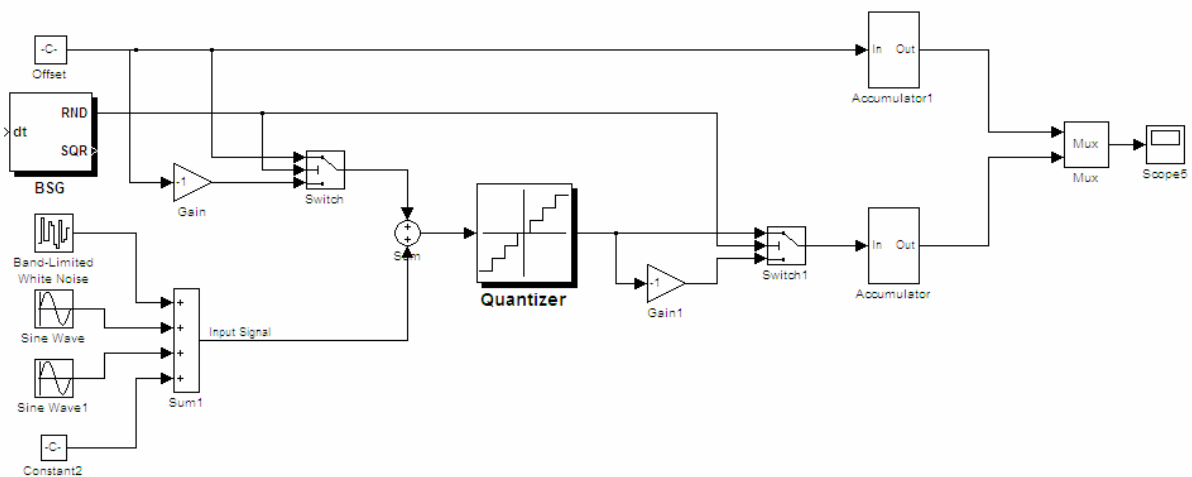


Figure 5: block diagram of the proposed on-line offset calibration scheme.

4 CONCLUSIONS

In this paper, a method for precise measurement of the *ADC* offset is proposed. The basic idea is to introduce suitable random modulation by +1 or -1 of the input signal. In our case, the modulating signal is the wide-band output of a Chua's circuit passed through a comparator. Simulations of the proposed approach at the behavioral level confirm the effectiveness of the method allowing the offset to be measured with an accuracy better than $2 \cdot 10^{-3}$. It is shown that the offset of a 12-bit *ADC* can be measured with a 0.1 LSB accuracy.

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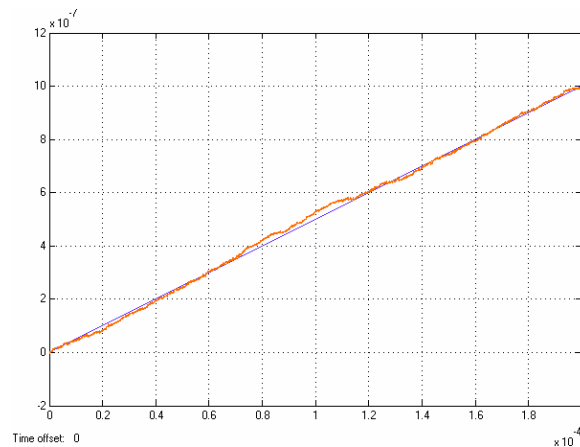


Figure 6: offset measure: offset integral (ϵ_{dc} black line), measured offset ($\epsilon_{dc,meas}$ grey line).