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A 14-BIT 20-MSAMPLES/S PIPELINED A/D CONVERTER WITH DIGITAL BACKGROUND CALIBRATION

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ABSTRACT

This paper describes a 14-bit 20MSPS switched-capacitor pipelined ADC that employs digital background calibration to correct capacitor mismatch. The calibration concept is amenable to implementation in SOC because it is digital in nature. The calibration concept is demonstrated offline though in principle it can be included on-chip. The calibration can also be performed periodically, thus is inherently able to track the operating conditions of the device. Implementation is in a complimentary bipolar process. The prototype exhibits typical INL of ±0.2 LSB, DNL of ±0.4 LSB, SNR of 73 dB and SFDR of 85 dB with a 2MHz input signal. Analog power is about 500mW with 5V supply.

1. INTRODUCTION

The current trend in VLSI system integration is the continued shift from signal processing in the analog domain to signal processing in the digital domain. This is driven by the scaling of advanced semiconductor processes and the ability to perform complex operations in the digital domain typically using DSPs, which are easily reconfigured via software. This has in turn spawned system-on-a-chip (SoC) circuits due to the unprecedented levels of integration possible. As a result, new methodologies and approaches are needed to address design, verification and test problems presented by SoCs in this rapidly evolving area. In data conversion, this trend has placed challenging specifications on the high performance ADC, which straddles the interface between the analog and digital domains. Low power yet high dynamic range designs are the preferred trend in order to ease thermal management and reduce system footprint [1]. ADCs for applications such as wideband digital communication systems need excellent SNR to avoid losing the weak signal in the quantization or thermal noise. They also require high spurious free dynamic range (SFDR) to avoid masking the weak signal with distortion artifacts from the stronger signal. These ADCs are also required to have resolutions in excess of 12 bits and signal bandwidths from 1 MHz to 100MHz. The pipelined ADC architecture lends itself well to this kind of applications but may require calibration to enhance integral nonlinearity.

In this paper, we design and apply digital background calibration on a pipelined ADC in order to improve linearity at the 14 bit level. It is well known [2] that the major limitation to high linearity of such devices is due to mismatch in the unity elements (capacitors) of the inter-stage Multiplying Digital-to-Analog converter (MDAC). The linearity of these elements is also critical for achieving harmonic distortion specifications, especially for the first stage of the pipeline. Traditionally, there are several approaches to improve the accuracy of the MDAC. They can broadly be lumped into two categories: Analog element calibration [3], [4] and digital calibration [5], [6]. Analog element calibration or trim corrects the ADC by adjusting the elements in the analog domain. It has two main drawbacks. First, for the case of one time element trim [4], variations in matching with temperature, power supply fluctuation, aging and so on may degrade the calibration. Second, methods such as laser trimming or fuse blowing not only add significantly to the cost of an IC but they may not readily scale with modern process nodes.
2. DIGITAL CALIBRATION

Figure 1 shows the general form of a pipeline converter. During each step of the conversion, a certain number of bits of the digital output are resolved. The most significant bits are resolved first; a residue (or remainder) is generated and passed down to the succeeding stages. Therefore each stage is responsible for resolving some segment of the digital output word. The primary advantage of the pipeline architecture [2] is that the inherent concurrence of operations results in a converter with a conversion rate that is limited only by the time it takes to process the analog information in one stage. In general, each pipeline stage implements a sample-and-hold operation, an A/D conversion, a D/A conversion, a subtraction, and amplification.

A detailed description of the calibration concept implemented in this work can be found in [7]. The calibration method employs an extra element in the MDAC and a master reference one. An extra element is included so that while another element is under calibration, the rest of the elements continue performing normal A/D operation without interruption. Each element (including the extra one) is sequentially placed in calibration mode, the mismatch between the selected element and the reference is then estimated and stored in a digital memory from which the INL at each code can be obtained. This INL is then subtracted from the overall converter output to perform calibration. A look-up table whose address is the output of the sub-ADC of the stage under calibration provides the value to be subtracted. In this method, each calibration session requires a relatively large number of clock periods.

![Diagrams](image)

**Figure 2a) and 2b)—Conventional and modified 2-bit switched capacitor residue generators respectively.**

To help explain the concept, Fig.2 a) shows a single-ended version of a switched capacitor residue generator incorporating a 2-bit DAC as commonly employed in a conventional pipeline. During phase 1, all the capacitors sample the input signal; during phase 2, by a proper control of three switches, one capacitor is connected around the op-amp and the rest are switched to the appropriate reference voltages. The capacitors C_{n,1}, C_{n,2}, C_{n,3} and C_{n,4} are nominally equal. Assuming that C_{n,4} is connected in feedback, the generated residue is,

\[ v_{\text{Re},1} = \frac{1}{C_{n,4}} \left( [ C_{n,1} + C_{n,2} + C_{n,3} + C_{n,4} ] V_{\text{in}} - \right. \]

\[ - C_{n,4} V_{\text{ref},1} \]  

\[ - C_{n,4} V_{\text{ref},2} - C_{n,4} V_{\text{ref}} \]

where \( V_{\text{ref},1}, V_{\text{ref},2}, V_{\text{ref},3} \) are the reference voltages applied to \( C_{n,1}, C_{n,2}, C_{n,3} \) during phase 2 respectively.

Fig. 2 (b) shows a modified version suitable for the calibration method. We have an additional capacitor \( C_{n,5} \) and \( C_{\text{ref}} \) reference capacitor. The capacitor in the calibration mode is switched between \( V_{\text{ref}} \) and \(-V_{\text{ref}}\) with a clocking scheme complementary to the one used for \( C_{\text{ref}}\); the other capacitances operate exactly as the ones in the conventional counterpart. Assuming that \( C_{n,5} \) is in calibration mode and that it is charged at \( V_{\text{ref}} \) during phase 1 (\( C_{\text{ref}} \) is meanwhile being charged at \(-V_{\text{ref}}\)), the residue voltage becomes,

\[ v'_{\text{Re},1} = \frac{1}{C_{n,4}} \left( [ C_{n,1} + C_{n,2} + C_{n,3} + C_{n,4} ] V_{\text{in}} - \right. \]

\[ - C_{n,4} V_{\text{ref},1} + \left. V_{\text{ref},2} - C_{n,4} V_{\text{ref}} \right) \]

This is the conventional residue voltage plus a term that depends on the mismatch between \( C_{n,5} \) and \( C_{\text{ref}}\). If \( C_{n,5} \) is in calibration mode and is charged at \(-V_{\text{ref}}\) during phase 1 the sign of the additional term is reversed. It is noted that the calibration would sequentially cycle through all the capacitors. This would happen without interrupting the normal operation of the converter. Equation (2) can also be expressed as,

\[ V'_{\text{Re},1} = V_{\text{Re}} + \frac{(C_{n,5} - C_{\text{ref}}) \cdot V_{\text{ref}}}{C_{n,4}} \]  

(3)

again, (3) is the conventional residue superimposed with a term proportional to capacitor mismatch. The main principle of this calibration method is to extract the mismatch term from the conventional residue by employing correlation techniques [7, 8]; the extracted mismatch at each code in the stage being calibrated is then subtracted from the overall ADC output. The switching scheme employed in the capacitors under calibration can be determined in a pseudo-random manner.

3. ADC DESIGN

The prototype ADC implemented in this work includes a front-end Sample and Hold (S/H) stage followed by six pipelined conversion stages that each resolve 3 bits except for the last 4 bit flash sub-ADC. Only the first stage is calibrated. The inter-stage gain is nominally 4. One bit of redundancy is used in each stage to facilitate digital error correction of stage sub-ADCs (flash comparator) errors [9]. Figure 3 shows a block diagram of most of the ADC. The complete circuit also includes a clock buffer, voltage reference and master bias current generator integrated on chip.
The choice of the number of bits resolved by each stage is a trade-off between power, component matching, SNR target and area.

Figure 4 shows the complete overview of the calibrated ADC. The front end S/H is a ‘flip-around’ bottom plate sampling type [11] as shown in Figure 5. It is designed to acquire a wideband input signal, drive the load of the first stage and relax the design requirements of the first-stage sub-ADC and residue stage by producing a sampled and held signal. It acquires the input on the capacitors during the track phase (P1), and flips the same capacitors to the output during the hold phase. The switches S1A and S1B are implemented with bootstrapped NMOS switches in order to improve their linearity [8] and thus reduce the harmonic distortion. All the other switches are implemented with CMOS transmission gates. The precision capacitors are integrated in trinitride-oxide-poly.

A schematic of the fully differential 3-bit first residue stage is shown in Figure 6. It has a nominal gain of 4. It operates on two phases, a sampling phase and a hold phase. During the sampling phase, the input signal is sampled on eight capacitors while the reference capacitors and the ones being calibrated are differentially switched between positive and negative references. During the hold phase, the capacitors are differentially switched to the reference voltages or shorted together. The reference voltage is selected in the conventional manner based on the digital output of the stage sub-ADC codes in order to generate a residue. (It is pointed out that the rest of the pipelined stages are similar to stage 1 except they do not have the extra capacitors and switches required for calibration). The residue is then gained up and passed on to the next stage of the pipeline converter. This process is repeated until all the bits are resolved. The accuracy requirements of each stage are relaxed by the amount of inter-stage gain preceding it.

The design approach adopted is based on obtaining a high SNR and sampling rate. The SNR for a pipelined ADC referenced to unity full-scale signal range can be approximated as [10],

$$\text{SNR} = 20 \log \left[ \frac{(2 \pi f_m t_i)^2}{2} \right] \frac{1}{2} + \left( 1+e \right)^2 + \left[ \frac{\text{V}_{\text{noise}}}{2^N} \right]^{1/2} \quad (4)$$

where, $f_m$ is the analog input frequency, $t_i$ is the rms aperture uncertainty, $e$ is rms DNL of the converter and $V_{\text{noise}}$ is converter electronic noise.
Consider the total input referred thermal noise in the ADC [11],
\[
d_{t_{\text{total}}}^2 = d_{t_{\text{H}}}^2 + d_{t_{\text{T}}}^2 + \frac{d_{t_{\text{G}}}^2}{G_1^2} + \frac{d_{t_{\text{G}_2}}^2}{(G_1G_2)^2} + \ldots + \frac{d_{t_{\text{G}_N}}^2}{(G_1G_2\ldots G_N)^2}
\] (5)

where \(d_{t_{\text{i}}}\) is the RMS thermal noise and \(G_i\) is the inter-stage gain of the \(i\)th stage respectively. The Sample-and-Hold (S/H) contribution is indicated by the subscript in (5). Total electronic noise is the orthogonal summation of the kT/C noise and amplifier noise assuming they are uncorrelated. For a fully differential implementation [12],
\[
d_{t_{\text{f}}}^2 = \frac{1}{C_T} \frac{2kT}{f^2} + V_{\text{opamp}}^2
\] (6)

where \(C_T\) is the total capacitance in the sampling phase and \(f\) is the feedback factor. \(V_{\text{opamp}}\) will depend on amplifier type (e.g., single-stage, multi-stage, etc) technology and design trade-offs. For bipolar devices, the base resistance \(R_B\) must be kept low to reduce amplifier thermal noise. Equations (5) and (6) are used to extract a value of \(C_T\) which meets a desired noise target. The above procedure was used to determine the 10pF sampling capacitors for this design in order to diminish the kT/C thermal noise floor to less than -80dB with a full-scale input voltage of 4Vpp.

4. EXPERIMENTAL RESULTS

In the test setup, the sinusoidal input to the prototype ADC is synchronized to the clock signal input. Both signals are coupled through RF transformers. The transformers convert the signals from single-ended to fully differential. A center tap also provides a means to set the desired common mode level. Digital calibration was performed on the data in MATLAB™. Code density test [13] method was used to determine the linearity. The underlying principle is that the transfer characteristic of an ADC can be measured with a known waveform applied as input. In this test, a large number of samples of an input signal are collected and converted to digital codes. Then the number of occurrences of each digital code is plotted on a histogram of frequency of occurrence versus code. If enough samples are taken, the effects of noise are averaged out and all of the information about the transfer characteristic of the ADC can be obtained.

As shown in Figure 7, the peak un-calibrated INL of the converter is approximately 4 LSB. With the calibration on, the peak INL is approximately 2.5 LSB. Therefore the ADC linearity is improved by 1.5 LSB. The residual INL is mainly due to finite DC amplifier gain, non-linear charge injection and nonlinear reference voltage effects. The signal-to-noise ratio was calculated by collecting 65536 samples and performing a FFT. This test was performed at sampling frequency of 20 MHz and an input frequency of 2 MHz set at -1 dBFS. The top portion of figure 8 shows the typical measured uncalibrated spectrum. The bottom figure shows the typical calibrated spectrum after calibration algorithm is performed. There is an improvement in SNDR of 3.36 dB.

Figure 7. Measured (a) INL and (b) post calibration INL at 14 bits, sampling rate of 20 MHz, input frequency 100KHz.

Figure 8. Typical FFT spectrums of a 2MHz input signal sampling at 20 MHz.

Figure 9. Chip micrograph.
Table. 1 Performance summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>14 bits</td>
</tr>
<tr>
<td>Sampling rate</td>
<td>20MSPS</td>
</tr>
<tr>
<td>INL/DNL</td>
<td>+/-2.0LSB, +/-0.5LSB</td>
</tr>
<tr>
<td>SNR</td>
<td>73dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>85dB for 2MHz input</td>
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<tr>
<td>Analog Power/supply</td>
<td>500mW/5V</td>
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<tr>
<td>Input range</td>
<td>4Vp-p</td>
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<tr>
<td>Process</td>
<td>0.5uM SOI/DI, SiGe</td>
</tr>
<tr>
<td></td>
<td>complementary Bipolar</td>
</tr>
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5. CONCLUSION

A 14-bit 20MSPS pipelined ADC with digital background calibration has been summarized. Calibration is demonstrated offline though in principle it can be included on-chip. Prototype implementation shows improvement in linearity as a result of the proposed calibration technique.

6. REFERENCES


