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Dynamic Element Matching for Low-power ΣΔ Modulator with R-C based internal DAC

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Abstract—The use of internal resistive-capacitive MDAC in ΣΔ modulators requires a special dynamic element matching (DEM) approach. This paper proposes two modified versions of the DWA method capable to obtain very high linearity with a large number of quantization levels (16 or 32). The benefit of a 4-5 bit DAC enables very low OSR and the use of a second order modulator for the conversion of 8 MHz bandwidth with 10-12 bit of accuracy and very low power consumption. Extensive behavioral simulations verify the effectiveness of the proposed methods with element mismatches as large as 1%.

I. INTRODUCTION

The communication market evolves more and more toward mobile solutions with an increased use of data converter whose signal bandwidth is typically several MHz, the resolutions is 10-12 bit with a required SFDR in the 70-80 dB range.

The sigma-delta (ΣΔ) technique that was used for obtaining high-resolution, low-bandwidth analog-to-digital converters is more and more used for low-power high-bandwidth systems as using small OSR exploits the noise-shaping benefit without requiring power hungry speeds in the op-amps. The low-power goal is typically reached with a proper choice of the oversampling ratio, of the order of the modulator and of the number of bits of the quantization [1].

The optimum trade-off between oversampling, order and number of bits depends on the matching accuracy between passive elements realizing the internal DAC and the effectiveness of the dynamic element matching (DEM) method used to improve the DAC linearity. As known, the matching properties of both resistors and capacitors improve with the area of the unity elements [2]. For capacitances, increasing the area means augmenting the unity value with a consequent increase of the capacitive load and the power consumption. On the contrary, since an increase of the resistor area does not change the value, therefore the power consumption and speed of operation are unaffected.

This paper points at the use of resistor-capacitor based internal DAC in ΣΔ architectures for obtaining a large number of bits without increasing the total capacitance or requiring unfeasible low unity element. Since with many bits the DEM is a critical block, this paper studies effective solutions that can be used to correct the mismatch of a two-dimensional R-C array of elements.

II. MATCHING OF ELEMENTS

The DAC used in ΣΔ architectures is made by unity elements whose number equals the number of quantization intervals. The elements are often capacitors (Fig. 1) and for some schemes current sources. The mismatch between elements causes a non-linear DAC response that, for capacitances equal to \( C_l = C_u(1 + \delta_l) \) and \( \sum_{i=1}^{N} \delta_i = 0 \) is

\[
V_{out}(k) = V_{ref} \frac{k + \sum_{i=1}^{N} \delta_i}{N}
\]

where it is assumed that for converting the code \( k \) the DAC selects the first \( k \) elements and the capacitors are switched between 0 to \( V_{ref} \).

Fig. 1. Schematic representation of a capacitive MDAC.

The static non-linearity of a 1-D array is normally improved by dynamic matching [3]. A frequently used method is the data weighted algorithm (DWA) that uses sequentially the elements of the array by pointing at the first not used element: it is the starting point in the next clock period. Assume that during the \( n \)-th clock period the DAC uses the \( 1-k_1 \) elements, the \( k_{1+1}-k_2 \) during the period \( (n+1) \) and \( k_{2+1}-k_3 \) during the period \( (n+1) \). If \( k_3 < N \) the three errors give rise to

\[
\frac{V_{ref}}{N} \left[ z^{-2}\epsilon_n + z^{-1}\epsilon_{n+1} + \epsilon_{n+2} \right]
\]

\[
\epsilon_n = \sum_{i=1}^{k_1} \delta_i; \ \epsilon_{n+1} = \sum_{i=k_{1+1}}^{k_2} \delta_i; \ \epsilon_{n+2} = \sum_{i=k_{2+1}}^{k_3} \delta_i; \quad (2)
\]

that, remembering the condition \( \sum_{i=1}^{N} \delta_i = 0 \), becomes

\[
\frac{V_{ref}}{N} \left[ (z^{-1} - z^{-2})\epsilon_n + (1 - z^{-1})\epsilon_{n+2} + z^{-1}\epsilon_{res} \right]
\]

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where $\epsilon_{res} = \sum_{k=1}^{N} \delta_k$ is a residual error that is possibly shaped in successive clock periods but with a reduced effectiveness. On the contrary the errors $\epsilon_n$ and $\epsilon_{n+1}$ are both shaped by a first order function.

The above study shows that the cyclic use of elements grants an effective shaping of the mismatch errors if the elements are entirely used in two or three clock cycles. Possible reminder are shaped less effectively especially for long reminder cycles.

**III. DAC DESIGN FOR LOW-POWER**

The use of multi-bit quantization is power effective because the bits used in the quantization reduce the oversampling ratio. It is therefore convenient to allocate part of the power budget for increasing the number of comparators for obtaining a net benefit in the the op-amps power reduction.

However, many bits can be problematic for the DAC architecture and the DEM. A DAC for medium resolution modulators should use the smallest capacitance permitted by the reference voltage, the desired SNR and the oversampling ratio. Remind that the $kT/C$ limit is

$$\frac{kT}{C_s} \frac{1}{OSR} < \frac{V^2}{2} 10^{-SNR/10}$$

that for $V_{ref} = 1V$, $OSR = 10$ and $SNR = 72dB$ gives for example $C_s > 138fF$. Since the technology permits designing minimum unity capacitances of about $25fF$, a capacitive DAC with more than 6 elements would lead to a total capacitance larger than the minimum allowed by the $kT/C$ constrain, leading to a quadratical increase of the power consumption as the transconductance gain is proportional to the capacitance.

The total capacitance is kept at a low value by using a resistive-capacitive DAC as shown in Fig. 2. The fractional values of $V_{ref}$ made available by the resistance divider increase the number of bits without increasing the total capacitance. Moreover, the power consumed by the resistive divider is negligible with, for example, $\tau = 5\mu s$ required time constants. If the used capacitance is $C_s = 0.2pF$ the total resistance of the array must be $R_T = R_0 = 50k\Omega$ that with $V_{ref} = 1V$ leads to a $20\mu A$ consumed current.

**IV. DYNAMIC ELEMENT MATCHING FOR R-C DAC**

We have discussed the benefit of using an $R-C$ DAC for medium resolution $\Sigma\Delta$ modulator. Since the accuracy depends on both resistor and capacitor matching, it is necessary to possibly use a dynamic matching technique that accounts for the 2-dimension array used by the DAC. For this the dynamic matching techniques are defined as 2-D.

This paper discusses two methods: the 2-D DWA IS (Immediate Shaping) and the 2-D DWA method. Both works well as they obtain a good shaping of the mismatch errors thanks to a direct or indirect multiplication of the error by $(1-x^{-1})$.

**A. 2-D DWA IS (Immediate Shaping)**

The DWA method used for a 1-D array of elements obtains a good shaping of the mismatch error as verified above. The extension of the resolution by a resistive divider foresees the switching of some unity capacitors from 0 to $V_{ref}$ for converting the MSB and one unity capacitance from 0 to $kV_{ref}/2^{n}$ for obtaining one of the $2^n$ levels of the LSB. The possible mismatch between resistors gives rise to an error.

In order to obtain an immediate shaping it is necessary to inject the inverse of the error at the next clock cycle. This is obtained by returning to zero the connection of the capacitance that has just been used to convert the LSBs. For doing this, as represented by Fig. 3, is necessary to add the previous LSB to the input signal before the new splitting in MSB and LSB. Therefore, the immediate shaping technique requires using an index for identifying the capacitance used with the resistive divider for converting the LSBs, and the one used for the same function one clock period before. The choice of the new index and the use of the remaining elements is determined by the dynamic element matching algorithm used for the remaining capacitances. The simulations used in this paper are based on the DWA algorithm.

![Fig. 3. Schematic representation of the R-C DEM with immediate Shaping.](image)

Assume that at the time $nT$ the input is $X(nT) = X_{MSB}(nT) + X_{LSB}(nT)$ and that at $(n+1)T$ the input is $X(nT+1)$. The DAC at $(n+1)T$ is controlled by

$$X_{out}(nT+1) = X_{out}(nT+1) + X_{LSB}(nT)$$

that gives rise to new MSB and LSB while the second term is compensated for the return to zero of the capacitor used for the previous LSB.

If the system uses the DWA algorithm the capacitor for the LSB is the last used capacitance for the previous MSB. Therefore, the index used is not affected by the immediate
LSB shaping. If the DWA index does not change (MSB=0), for the next LSB it is necessary to go back by one position as the MSB does not use any element as required for accommodating the new LSB.

A drawback of the approach is that the number of unity elements must increase by two as it is necessary to compensate for the return to zero term. It is possible to have only one extra element but the logic must be more complicated for being able to convert input data close to the full scale.

B. 2-D DWA

The immediate shaping method obtains the result (as also verified by behavioral simulations) but requires a fairly complex logic. The 2-D DWA algorithm described below obtains almost the same benefits with a simpler digital control.

We have seen in the Section II that the first order shaping of a 1-D array is ensured if the entire array is exercised in two or three clock periods. A possible residual error gives rise to an extra term that can be possibly shaped but in a less effective manner.

The 2-D DWA method exploits the above mentioned feature by using a 2-D rotation of the resistive and capacitive elements.

Assume that the input data of a 4-bit (2+2) R-C DAC is $10$. Therefore, the logic will use two capacitors sampled at the reference voltage and one capacitor sampled at $2V_{ref}/4$. Since the DAC uses completely two capacitors of the array and only partially the third capacitor, it is necessary to complete the use of the third element during the next clock period. Since the partially used capacitance can contribute with only a fraction of its maximum, an input data close to the full scale cannot be converted unless using an extra unity capacitance that is beneficial because brakes possible repetitive patterns at half of the full scale but, worsening the feedback factor, requires more power. The limit is acceptable for an increase from 4 or more unity elements.

Fig. 4 shows the control scheme of the one of the R-C elements of the DAC. Two of the switches connected to the resistive divider are operated by the phase 1 or the phase 2 giving rise to an injected charge proportional to the difference between the voltages of the connections during phase 2 and phase 1.

.png

Fig. 4. Control scheme of a capacitor element of the DAC with R-C DWA algorithm.

V. ERROR SHAPING

In the proposed methods the total mismatch error for each configuration comes from the sum of the error introduced by the kelvin divider and by the capacitor network. The charge that is injected in the integrator when the $n$-th resistor is connected to the $m$-th element of the capacitance network is:

$$ Q_{nm} = \frac{2V_{ref}}{\sum_{k=1}^{N_R} R_{km}(1 + \varepsilon_{R_k}) C_m(1 + \varepsilon_{C_m})} $$

$$ n = 1, 2, ..., N_R; \quad m = 1, 2, ..., N_C; $$

where $N_R$ and $N_C$ are the number of elements in the resistive divider and in the capacitive network respectively and $\varepsilon_{R_k}$ and $\varepsilon_{C_m}$ are their relative mismatches. Assuming the condition that the average error is zero, then:

$$ \sum_{n=1}^{N_R} \varepsilon_{R_n} = 0; \quad \sum_{m=1}^{N_C} \varepsilon_{C_m} = 0; $$

Thus, (6) can be re-written as:

$$ Q_{nm} = Q_u(1 + \varepsilon_{R_n})(1 + \varepsilon_{C_m}) $$

$$ = Q_u(1 + \varepsilon_{R_n} + \varepsilon_{C_m} + \varepsilon_{R_n}\varepsilon_{C_m}) $$

$$ \approx Q_u(1 + \varepsilon_{R_n} + \varepsilon_{C_m}) $$

Fig. 5 shows the conceptual schematic representation of the proposed algorithms for a 16-bit (4+4) R-C DAC. The picture highlights that the proposed approaches have the same behavior of a standard DWA algorithm. The unity amount of charge that is injected into the integrator comes from the sequential combination of the selected capacitors with the resistors cyclically connected, thus the mismatch errors derive from the mismatch contributions of both resistors and capacitors.

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Fig. 5. Conceptual representation of R-C and IS DWA algorithm.

VI. SIMULATION RESULTS

A second order $\Sigma\Delta$ Modulator (Fig. 6) is implemented to demonstrate the effectiveness of the proposed new algorithms. It is a 16 level quantization ADC with an oversampling ratio of 16. The DEM algorithm is applied to the feedback networks of the two stages. The used mismatch errors are
an improvement in the signal to noise ratio of the whole system.

Fig. 6. Second Order $\Sigma\Delta$ Modulator with DEM algorithm.

1% and 2% for capacitors and resistors respectively. Fig. 7 shows the DAC errors for the R-C and IS DWA algorithms. As expected, the DWA algorithms have a first order shaping of the mismatch error. Fig. 7 and Fig. 8 illustrate that in absence of a DEM algorithm the mismatch error in the DAC produces an increase in the floor noise and tones in the signal bandwidth. For this case a reduction of about 3 bits in the SNR of the $\Sigma\Delta$ Modulator is obtained. Fig. 9 and Fig. 10 show the $\Sigma\Delta$ Modulator output spectra when the DWA algorithms are operating in the internal DAC. In both cases the algorithm cancels the tones in the signal bandwidth allowing

Fig. 7. PSD of the mismatch error in the architectures with no DWA algorithm, with R-C DWA and with IS DWA.

Fig. 8. Output spectrum with no DEM algorithm.

VII. CONCLUSION

The use of internal resistive-capacitive MDAC in $\Sigma\Delta$ modulators with a special dynamic element matching (DEM) approach allows obtaining very high linearity with a large number of quantization levels (16 or 32). The benefit of a 4-5 bit ADC enables very low OSR and the use of a second order modulator for the conversion of 8 MHz bandwidth with 10-12 bit of accuracy and very low power consumption. The choice of the proper architecture depends on a trade off between effectiveness of the error shaping technique and circuit complexity.

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