DTMF Generator based on Interleaved Oversampling

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Abstract: A circuit is described which uses one oversampling frequency synthesizer in an interleaved mode to generate dual-tone multi-frequency (DTMF) telephone dialling tones. The synthesizer is based on direct digital synthesis using phase accumulation. The digital to analogue conversion is carried out using a first order sigma–delta (ΣΔ). This ΣΔ converter is also used in interleaved mode. The smoothing filter consists of a simple second order RC filter.

1. Introduction.

Designing a DTMF generator in 1989 may seem like reinventing the wheel, but the market for telephone dialler chips is still sufficiently large that, finding new solutions to this problem with smaller silicon area and better performance is still of great interest. Optimized frequency synthesizers are also of interest because of their wide area of application in modems, telephone ringing, clock generators etc.

Previous solutions for the DTMF generator use either switched capacitor [2] or resistor string synthesizers [3] with one synthesizer per frequency group. These synthesizers use oversampling ratios in the range from 8 to 16, resulting in mirror frequency components relatively near the base band. This requires the use of precision smoothing filters to remove the unwanted frequencies. Conventionally these filters are constructed using a switched capacitor filter, followed by an RC smoothing filter.

The DTMF generator proposed here uses only one synthesizer in an interleaved mode to generate both frequencies. The synthesizer is based on direct digital synthesis [5,6]. An oversampling rate of approximately 1000 is used. This prevents the problem of mirror frequency components near the base band and permits the use of a simple first order sigma–delta digital to analogue converter.


The specification for DTMF dialling were standardized by the CCITT in 1968 [1]. The required tones are given in table I. All frequencies must be generated with an accuracy of 1.5%.

<table>
<thead>
<tr>
<th>High Frequency Group</th>
<th>Low Frequency Group</th>
</tr>
</thead>
<tbody>
<tr>
<td>f\text{ideal}</td>
<td>f\text{gen}</td>
</tr>
<tr>
<td>1633</td>
<td>1638.7</td>
</tr>
<tr>
<td>1477</td>
<td>1474.9</td>
</tr>
<tr>
<td>1336</td>
<td>1338.3</td>
</tr>
<tr>
<td>1209</td>
<td>1215.4</td>
</tr>
</tbody>
</table>

Table 1. Required Frequencies, Generated Frequencies and % Error

Fig 1. shows the architecture of the new DTMF generator. The two registers R1 and R2 contain the phase increments necessary to generate the two required frequencies. The output of these registers are loaded alternately into the accumulator. The accumulator feedback register has been modified to a z–2 function, this together with the alternative loading of the input registers allows the incrementing of both phases in one accumulator. This data is then put through a sine ROM. The required pre-emphasis is obtained by alternating the weighting of the sine ROM by 0 dB and -2 dB (i.e. every second sample put through the ROM is weighted with -2dB ). The output of the ROM contains interleaved samples of both frequencies f1 and f2 with the required pre-emphasis.
By demultiplexing the output from the DAC it is possible to build a circuit with an unweighted sine ROM. Such a circuit has also been tested but rejected for two reasons. The area which can be saved in the digital circuit is required in the analogue section to build a filter with two inputs. Secondly measurements on the test circuit showed higher levels of intermodulation between the lower and upper frequencies than with the present solution.

To reduce the requirements on the smoothing filters it was decided to run the frequency synthesizer with as high frequency as practical. In this case, the increment frequency used is 1.79 MHz, giving mirror frequencies in the mega hertz range. The filter required to remove these frequencies is a simple second order RC filter, which does not have stringent requirements on corner frequency variations. This filter is significantly smaller in area than the previously used switched capacitor filters. An oversampling rate of 1000 also simplifies the digital to analogue conversion. The DTMF specification can be fulfilled using a simple first order sigma-delta converter [6]. The \(\Sigma-\Delta\) converter is also used in an interleaved mode. The one bit pulse stream from the DAC is filtered using a second order Sallen and Key filter which also functions as the output buffer. The simulation results and the specification for the complete circuit are shown in figure 2.

3. Implementation.

To generate the frequencies with the required accuracy a 16 bit accumulator is necessary. This can be calculated using equation 1 and the required frequencies from table 1. The register values needed to generate each frequency are also given in table 1. Calculations indicated that the sine ROM only needs a 5 bit address and 4 bit data, making it extremely small. The \(\Sigma\Delta\) digital to analogue converter is constructed in the manner proposed by J. Candy [6] using a simple accumulator circuit. The accumulator has been modified to run in an interleaved mode; this reduces the dynamic range required and the maximum effective frequency seen by the digital to analogue converter.

\[
F_{\text{out}} = \frac{\text{Reg Data}}{2^n} \cdot F_{\text{clk}} \quad \text{eqn. 1.}
\]

Where: \(F_{\text{clk}}\) is the clock frequency used.

\(n\) is the number of bits in the accumulator.

The output bit-stream from the \(\Sigma\Delta\) digital to analogue converter, is filtered using a Sallen and Key low-pass filter. This structure has been chosen, because this allows the use of well-resisters when integrating the filter, without causing harmonic distortion in the passband.

To enable a fastest possible verification of the concept, it was decided to use a standard cell approach for the layout (see figure 3). The sine ROM is implemented using standard gates, this is to facilitate an automatic routing and placement. For the full custom layout, a custom ROM is being made storing only 90\(^0\) of the sine function. The synthesizer requires 1.5 mm\(^2\) in 2 \(\mu\)m CMOS using a standard cell
layout. Present work on a full custom layout indicates that an area less than 0.5 mm² is achievable. The bit-slice nature of the circuit is very suitable for a full custom layout.


Measurements on the circuit confirm that all specifications of the DTMF [1] are fulfilled. Figure 4 shows a measured spectrum from 0 to 10 KHz. Figure 5 shows a measured spectrum from 0 to 100 KHz. The measured and simulated results show a remarkable correspondence.

5. Acknowledgments

We would like to thank Peter Lee and Oluf Alminde for many helpful discussions during this work.

6. References.


Figure 2: Complete circuit simulation.

Figure 3: Standard cell layout.

Figure 4: Output Spectrum 0 – 10 KHz

Figure 5: Output Spectrum 0 – 100 KHz