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An 11 Bit Sub-Ranging SAR ADC with Input Signal Range of Twice Supply Voltage

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Abstract—Analog-to-digital converters are one of the essential components in modern highly integrated Power Management ICs (PMICs). Although, the conversion time and resolution requirements are relatively easy to achieve, the requirements such as extended input signal range exceeding the system supply level, low power consumption for higher system efficiency, and resilience to heavy substrate and supply noise complicate the design of the ADC. In this paper, an 11 bit Sub-Ranging SAR analog to digital converter designed for power management systems is presented. The supply voltage and the reference voltage of the converter are both equal to 2.75 V while any of its 8 input channels can vary between 0 - 5.5 V range (or twice the reference voltage). The integral and differential nonlinearities of the converter are 0.38 and 0.45 LSB respectively. The ADC draws only 140 μ A of quiescent current and has a conversion time of 10 μ s.

I. INTRODUCTION

Modern highly integrated power management ICs (PMICs) employ analog-to-digital converters for sensing temperature, battery gauge levels, and to monitor on-chip and off-chip voltage levels, as well as perform basic signal processing [1]. Typically, the ADC is a low-power multi-channel SAR converter with conversion times ranging from tens of microseconds to hundreds of milliseconds, and resolutions varying from 8 to 11 bits.

Since these converters are used mostly for monitoring and supervisory purposes, static linearity (INL and DNL) and absolute accuracy (offset and gain errors) are the most important performance parameters.

Advanced PMICs require proper operation with a wide range of battery voltages. The ADC should be able to convert input signals while running from very low supply voltage levels and still precisely measure off-chip voltage quantities that can be significantly higher than its supply. The above described situation is challenging because it requires not only to switch voltages that can be higher than the used supply but also to perform the basic operations needed to implement the conversion algorithm like the subtraction of voltages [2].

In addition to the low-power and extended input signal range requirements, PMIC ADCs should be very resilient to substrate and supply noise typically generated by high power switching regulators present on the PMIC.

The switching of a voltage higher than the supply level is made possible by using a special bootstrapping technique, shortly recalled below [3], [4]. This paper describes other

design techniques that make possible the design of an 11 bit Sub Ranging ADC made by a first 1-bit stage followed by a 10-bit SAR ADC. The ADC's input signal range is twice the supply voltage and after the first stage the signal range is bounded by the supply. This is achieved without any input signal conditioning or loading of the input. The ADC is implemented in a twin-well 0.35 μ m CMOS technology with high voltage power device capability.

The work in this paper is organized as follows: Section II presents an overview of the proposed ADC architecture and summarizes system level design requirements. Section III discusses the implementation of the various sub-blocks employed in the ADC architecture, Section IV summarizes the measurement results of our proposed ADC, and finally section V is reserved for the conclusion and recommendations drawn from this work.

II. ARCHITECTURE OF PROPOSED ADC

Classical approaches for measuring input signals exceeding supply voltage all involve attenuating the input signal and performing the measurement/conversion on a scaled-down version of the input signal that is bounded within supply rails [5]. This attenuation is undesirable for the following reasons: a) The attenuator would load the input signal and not all input signals can maintain their integrity when loaded b) the accuracy of the conversion degrades severely due to the errors introduced by the attenuator, and c) for a given converter resolution, attenuating the input signal results in smaller LSB levels which will be even harder to resolve in the noisy environment of PMICs.

Fig. 1. Proposed 11 bit Sub-Ranging Analog to Digital Converter

The design challenge is to realize an ADC with $0 - 2V_{ref}$ input signal range without using attenuation. Note that the reference voltage and the supply voltage of the system are equal. The circuit whose architecture is shown in Fig. 1 obtains the result. The first part of the scheme operates at a voltage that can be higher than the supply for obtaining the MSB. The second section works within the supply range and determines 10 additional bits. The first part makes use of a high-voltage bootstrapped-switch (HVBS) that is capable of switching in an input signal exceeding the supply voltage without forward-biasing any parasitic body diode [3], [4]. The switches that realize the input channel multiplexer are all HVBS switches.

After the input mux, the first stage compares the input signal with V_{ref} . The result of this comparison determines whether the input signal is within the $0 - V_{ref}$ subrange or the $V_{ref} - 2V_{ref}$ subrange. Accordingly, this result corresponds to the MSB of the conversion. Subsequent to this decision, either the input signal itself (MSB = 0) or the difference between the input signal and V_{ref} (MSB = 1) is fed to the next stage. The operation of the first section is therefore equivalent to the first stage of a sub-ranging ADC with just one bit. Moreover, if the signal range of the entire ADC is $0 - 2V_{ref}$, the residual without interstage amplification can be bounded in the $0 - V_{ref}$ range enabling the use of a conventional ADC which in this design is a 10-bit SAR.

The scheme confines all the challenges related to the processing of the high voltage input signals, i.e. reliability and the parasitic body diodes, to the first stage. The key problem is to generate the residual of the first stage that equals to the input or to the input minus V_{ref} in the case the input exceeds V_{ref} . The operation is made possible by the novel high-voltage passive subtractor described in the next section. The subtractor, which must have a resolution better than 10-bit, provides a residue that is twice the one of counterparts with input signal attenuation. Therefore, the double LSB enables a better rejection of spurs and, in turn, a higher ENOB.

The second stage of the converter is implemented as a 10 bit SAR ADC. The SAR converter uses two 5-bit binary arrays capacitors. The value of the used attenuating element is rounded and causes a systematic error that is corrected in the digital domain. The issue is addressed in more detail in the next section.

III. SUBBLOCKS

A. High-Voltage Bootstrapped-Switch (HVBS)

An input voltage exceeding the supply can be switched on and off reliably using the circuit shown in Fig. 2. This bootstrapped switch utilizes a charge pump to charge C3 to V_{dd} during the OFF phase. During the ON phase, the switch biases the gate of MN1 with the charged capacitance C3 connected between the input voltage and the gate of the bootstrapped NMOS, MN1. The switch avoids any forward biasing of body diodes and more information on the workings of the switch can be found in [3],[4].

Fig. 2. Schematic of High-Voltage Bootstrapped Switch

Fig. 3. Simplified Schematic of the High-Voltage Passive Subtractor

B. High-Voltage Passive Subtractor

Active circuit techniques cannot be employed to realize the subtraction operation described in section II. The reason is that the $0 - V_{ref}$ signal range of the residue would need using an active circuit with supply above V_{dd} and capable to generate 0 output. The solution used by this circuit is the passive implementation of Fig. 3 that obtains the subtraction by a suitable dynamic biasing of the bottom plate of C1 and the transferring of the result to C2. The structure has true rail to rail input and output capability, consumes no static power, but requires multiple clock cycles to settle.

The detailed operation of the passive subtractor is as follows: First S1 is switched on to connect the top plate of C1 to the input signal V_{in} , while the bottom plate of C1 is charged to V_{ref} . Upon disconnecting the top plate of C1, the bottom plate is pushed to ground potential. As a result $V_{in} - V_{ref}$ appears across C1. Finally, S2 is turned on to connect N1 to the output capacitor, C2, which is the sampling capacitance of the second stage. The clock phases Φ_1 , Φ_2 and Φ_3 in Fig. 3 realize the aforementioned timing scheme.

Since the scheme of Fig. 3 is a passive switched capacitor RC, the output voltage approaches the final value with a time constant that depends on C1, C2 and the clock period used. Therefore, it is necessary to use a suitable number of cycles to achieve the desired accuracy. Moreover, the scheme is parasitic

sensitive resulting in a possible gain error and distortion. In order to keep the error below αLSB the value of C_1 must be chosen such that

$$C_1 > \left(\frac{2^{N-1}}{\alpha} - 1 \right) C_p \quad (1)$$

where C_p is the equivalent parasitic capacitance between N1 and ground. The condition is stringent but achievable with a careful layout of capacitances. The number of cycles m required for the passive subtractor to settle within an error less than αLSB at the output can be calculated as

$$m > \log_{(1+\frac{C_1}{C_2})} \frac{2^N - 1}{\alpha} - 1 \quad (2)$$

C. 10-bit SAR ADC

The use of a binary array of 2^{10} unity elements is impractical for the large required area and the large capacitive input load. This SAR ADC uses two arrays of 2^5 elements for a 5+5 bit segmentation.

To obtain ideal ADC transfer function, the value of the coupling capacitor should be fractional. Instead its value is rounded to the unit capacitance, C_U , for facilitating the layout of the entire capacitive array [6]. The choice gives rise to systematic offset error. Indeed, the realized transfer function is

$$\text{Out} = \text{int} \left(\frac{V_{in}}{\text{LSB}} \right) \quad (3)$$

where LSB is defined as $V_{ref}/1023$. Note that due to the systematic offset, the output reaches to the maximum code when the input signal reaches to V_{ref} .

The most significant 4 bits are transformed from binary to thermometric for controlling unary elements of the MSB array for ensuring monotonicity and improving the linearity.

D. Cascading the Stages and The Adder Block

The ideal transfer function of the 11 bit Sub Ranging ADC converter after cascading two stages can be expressed as follows:

$$\text{Out} = \begin{cases} \text{int} \left(\frac{V_{in}}{\text{LSB}} \right) & \text{if } V_{in} < V_{ref} \\ 2^{N-1} + \text{int} \left(\frac{V_{in} - V_{ref}}{\text{LSB}} \right) & \text{if } V_{in} \geq V_{ref} \end{cases} \quad (4)$$

This transfer function has a missing code appearing at the mid of the input range. This is due to following reason: As mentioned previously, the output of the 10 bit SAR ADC reaches to the maximum code only after the input signal reaches to the reference voltage level. The first stage, on the other hand, decides that the MSB bit is 1 and starts subtracting the reference voltage from the input at the very same input level, V_{ref} . As a result, the output code jumps from binary code 1022 to binary code 1024 while the input transitions from one subrange to the next.

Fig. 4. Die Photo of 11 Sub Ranging SAR ADC

Fig. 5. Measurement results of High-Voltage Passive Subtractor

An easy fix to this problem is to subtract 1 LSB from the output code if MSB bit is equal to logic 1. This way, the missing code at the middle of the input signal range can be shifted to the higher end of the transfer function. The adder block at the output of the ADC is exactly performing this task. Due to this subtraction, the ADC's number of obtainable output codes is 2047 instead of 2048 which is a very small price to pay compare to having a missing code at the mid of the input range.

IV. IMPLEMENTATION AND MEASUREMENT RESULTS

The ADC is implemented in a twin-well $0.35 \mu\text{m}$ standard CMOS technology with high voltage power device capability. Fig. 4 shows the microphotograph of the test chip. The silicon area of the 11 bit Sub-Ranging SAR ADC is $560 \text{ by } 560 \mu\text{m}^2$. The functional blocks are encircled and numbered within the die photo: 1) Input MUX, 2) High-voltage passive subtractor, 3 to 5) First stage comparator, switches and phase generator, 6) 10 bit SAR ADC and 7) Digital adder, test structures and digital interface circuitry.

The supply and reference voltage level of the converter are both 2.75 V. It draws 120 μA and 20 μA quiescent current

Fig. 6. Measured Differential nonlinearity of the ADC

Fig. 7. Measured Integral nonlinearity of the ADC

from the supply terminal and reference voltage terminal respectively. The conversion time is $10 \mu\text{s}$ with a system clock of 2 MHz.

Fig. 5 shows the measurement results of the passive subtractor. The input and the output signals are plotted on top of each other. From the reference pointers of the channels, the subtraction of DC V_{ref} from the input signal is apparent. Note also that the low pass characteristic of the blocks attenuates the ringing seen on the input signal at the output.

Measured DNL and INL characteristics of the 11 bits ADC are shown in Fig. 6 and Fig. 7. The DNL and INL of the converter are 0.45 LSB and 0.38 LSB respectively. The sudden jump of the INL curve at the mid of the input range, i.e. V_{ref} , is due to the error introduced by the passive subtractor circuit. Note that the INL curve of the 10 bit SAR ADC repeats itself within both subranges. Table I summarizes the performance of the proposed ADC.

TABLE I

PERFORMANCE SUMMARY OF 11 BIT SUB-RANGING SAR ADC

Parameter	Value	Unit
Supply Voltage	2.75	V
Reference Voltage	2.75	V
Input Signal Range	5.5	V
Input Signal Bandwidth	DC	Hz
Number of Input Channel	8	-
Conversion Time	10	μs
System Clock Frequency	2	MHz
Resolution	11	bit
LSB	2.688	mV
DNL	0.45	LSB
INL	0.38	LSB
Supply Voltage Current	120	μA
Reference Voltage Current	20	μA
Input Pin Current	5	μA
Silicon Area	560×560	μm^2
Technology	0.35 μm Twin-Well BCD CMOS	

V. CONCLUSION

An 11-bit sub-ranging ADC converter, capable of an input range equal to twice the supply voltage has been presented. The proposed ADC is a key element for integrated PMIC applications. The circuit avoids the input attenuators used for bringing the input within restricted signal ranges and obtains a significant advantage, as the large noise caused by switching mandates keeping the amplitude of the LSB as high as possible.

The described solution maintains the full swing of the input by using two key blocks: a bootstrapped switch capable of operating with an input at $2V_{dd}$ and a passive subtractor. The proposed circuit techniques have been demonstrated on silicon for obtaining an 11-bit ADC with 0.45 LSB and 0.38 LSB DNL and INL respectively proving targeted 11 bit linearity. The ADC consumes only $140 \mu\text{A}$ quiescent current and its conversion time is $10 \mu\text{s}$.

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