DESIGN AND EVALUATION OF AN INTEGRATED DIGITAL-ANALOGUE FILTER CONVERTER

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Abstract

This paper describes the design, integrated circuit implementation, and experimental evaluation of a novel building block that realizes the combined operations of digital-analogue conversion and FIR filtering (DAFIC). To maximize the advantages of both digital and analogue techniques, the circuit comprises a 4-stage digital delay line providing the input to 4 8-bit algorithmic digital-analogue converters whose gains are weighted according to the coefficients of an FIR filtering function. The circuit was implemented using a 3µm Single-Metal/Double-Poly CMOS process. Experimental results obtained from prototype chips are in good agreement with the expected theoretical behaviour of this novel building block.

1. INTRODUCTION

Modern integrated systems usually include digital as well as analogue functions in the same chip to reduce the total costs of manufacturing, and thus increase the commercial viability of the whole system [1]. This is particularly relevant in the development of interfaces between digital and analogue environments [2] where innovative concepts for mixed-mode signal processing are emerging to create more efficient structures from the standpoints of performance and silicon area. Recently, we have proposed a new building block which is capable of realizing simultaneously a W-bit Digital-to-Analogue (D/A) conversion together with a Finite Impulse Response (FIR) transfer function with arbitrary length N [3,4,5]. The filtering function is realized using a transversal structure where the delay line is performed in the digital domain whereas the weighting by the coefficients and the addition are both realized in the analogue domain simultaneously with the D/A conversion function. For this novel building block we have proposed several architectures which, depending on a specific application, can be selected on the basis of component count, capacitance spread, speed of operation and accuracy of the conversion and filtering functions [3,5]. To demonstrate the feasibility of such building block, we present in this paper the design, Integrated Circuit (IC) implementation, and experimental evaluation of an 8 bit/4 tap (W=8, N=4) DAFIC using a 3µm single-metal/double-poly CMOS process. Experimental results demonstrate the correctness of operation and good performance.

2. ALGORITHMIC DAFIC ARCHITECTURE

Algorithmic Digital-Analogue Converters (DACs) are usually utilized to minimize silicon area in applications where a lower speed of operation is not a limiting factor [6]. When such conversion technique is applied to the DAFIC, it leads to significant reductions in silicon area and circuit complexity in comparison with alternative techniques [5]. Fig.1 represents the general architecture of an algorithmic DAFIC. It comprises a digital delay line realized by serially associated shift registers, and an analogue output block where the delayed digital words are converted according to the coefficients $h_n$ (n=0 to N-1) of the FIR transfer function and added together. The output of the DAFIC, sampled just before phase $\Phi_R$ (Fig.1-a), can be expressed as

$$V_{OUT}(\omega) = \sum_{n=0}^{N-1} V_{OUT,n} z^{-n}$$

where $z^{-n}$ represents the delay factor of the input digital word associated with the SC branch with capacitance value $C_P$ (n=0 to N-1), and $V_{OUT,n}$ represents the corresponding converted analogue voltage. Such analogue voltage, in turn, results from the superposition of the output voltages produced bit-by-bit according to the conversion algorithm [6]. This process of conversion is carried out sequentially from the Least Significant Bit (LSB) $b_0$ to the most significant bit $b_{N-1}$, and it can be shown that at the end of the conversion period (Fig.1-d) the contribution of each bit is given by

$$V_{OUT,n}(b) = \pm \frac{C_n}{C_F} V_R 2^{W_i-n} b_i$$

where the sign of the coefficient depends on the switching of the input capacitor, as indicated in Fig.1-b and in Fig.1-c respectively for positive and negative coefficients. Therefore, the total contribution associated with one input SC branch alone can be written as

$$V_{OUT,n} = \pm \frac{C_n}{C_F} \sum_{i=0}^{W_i} V_R 2^{W_i} b_i$$

yielding, from (1), the following expression for the output voltage of the DAFIC
Fig. 1: a) General DAFIC architecture using an algorithmic D/A conversion technique, switching arrangements for b) positive and c) negative coefficients, and d) switching waveforms.

$$V_{OUT}(0) = \sum_{n=0}^{N-1} \frac{C_n}{C_F} z^{-n} \sum_{i=0}^{W-1} V_R 2^{-W+i} b_i$$ …(4)

The term $$\sum_{i=0}^{W-1} V_R 2^{-W+i} b_i$$ corresponds to the well-known binary-weighted implementation of a D/A conversion, whereas the term $$\sum_{n=0}^{N-1} \frac{C_n}{C_F} z^{-n}$$ corresponds to the implementation of an FIR filtering function whose tap coefficients are given by $$b_i = \frac{C_n}{C_F}$$ (n=0...N-1).

3. INTEGRATED CIRCUIT IMPLEMENTATION

The integrated circuit DAFIC was designed in order to implement a D/A conversion with 8 bit resolution and an FIR transfer function having 4 equally weighted taps and unity DC gain. This yields the transfer function H(z)=1/(1+z^{-1}+z^{-2}+z^{-3}) whose frequency response produces notches at F_s/4, F_s/2 and 3F_s/4.

Analogue Section: In Fig. 2 we present the folded cascode Operational Amplifier (OA) structure used in this IC implementation [7]. The W/L ratios are designed for a DC-gain of 70dB, a gain-bandwidth product of 7MHz and a settling time of 250ns. Compensation is realized by an appropriate minimum value of the capacitive load (C_C). The resulting simulated power consumption is only 670μW for a 5V power supply.

Fig. 2: Modified folded cascode amplifier.

The analogue switch cell, represented in Fig. 3, is realized using a pair of CMOS transmission gates. High-quality double poly capacitors are implemented as an association of C=0.25pF unit capacitors to improve the resulting capacitance matching [7]. The capacitance values are C_0=C_1=C_2=C_3=3C, and C_F=12C. For the resetting capacitor C_R, which is not critical, we adopted a capacitance value of 8C.
Digital Section: The digital circuitry is formed by $N=4$ serially associated dynamic shift registers with $W=8$ cells. The basic register cell is illustrated in Fig.4. At the end of the shift register there is an interface cell, shown in Fig.5, to control the switching of the input branch to the reference voltage.

Floorplanning and Layout Considerations: The chip floorplanning was carefully determined to minimize coupling of digital signals onto critical analogue lines. The chip employs independent power supplies to the digital and analogue sections, and the substrate under the analogue section is biased with a surrounding ring connected to the analogue $V_{DD}$ (N type substrate). This technique keeps the inner substrate at a nearly constant potential, thus preventing the propagation of digital spikes via the substrate. In Fig.6 we present a photomicrograph of the chip occupying a total silicon area of $1 \times 1.5 \text{mm}^2$ (PAD's included). In the layout of the OA, the MOS transistors are implemented in an interleaved form (stacked implementation) to improve matching. The capacitors are laid-out as an association of unit capacitors, and for capacitors $C_F$ these are also interleaved to maximize their matching [7].

4. PROTOTYPE CHIP TESTING AND EXPERIMENTAL RESULTS

The tests of the integrated circuit were carried-out using an experimental board containing all the circuitry necessary to generate the bias current and the biasing voltages for the OA, the appropriate switching waveforms and the conversion of the input data to the DAFIC from a parallel digital word into a serial digital word. The block diagram of the experimental board is presented in Fig.7, and it can be configured to measure either the linearity of the D/A conversion or the frequency response of the DAFIC.

Linearity Tests: The linearity of the D/A conversion was tested using only one tap of the DAFIC, a reference voltage of 1.8V, and a switching frequency of 20kHz for clock phases $\phi_1$ and $\phi_0$. In Fig.8 we present a plot of the conversion error obtained from the difference between the D/A conversion characteristic and the best adapted straight line. While the analysis of the plot shows that the error is always between ±0.6 LSB, the best straight line indicates a gain deviation of 2% from the theoretical value of 1/4, and an output offset of only -2mV, corresponding to 0.3LSB.

Frequency Response Tests: In order to evaluate the frequency response of the DAFIC, we utilized a 12 bit Analogue-to-Digital Converter (ADC) to generate the digital words to be serially applied to the DAFIC input. The reference voltage of the ADC was 5V, whereas in the DAFIC we utilized $V_R=0.5V$ and a switching frequency of 20kHz for $\phi_1$ and $\phi_0$. The frequency response measured from the input of the ADC to the output of the DAFIC is represented in Fig.9.a. The 20dB DC attenuation is due to the difference between both reference voltages. In Fig.9b we can compare both the theoretical and the experimental responses of the DAFIC, showing its correct operation.
5. CONCLUSIONS

In this paper we described the design, IC implementation and experimental evaluation of a novel building block that realizes the combined operations of D/A conversion and FIR filtering. The experimental results show the good performance of the circuit, leading to the conclusion that the DAFIC represents a good alternative to the classical solutions where D/A conversion and FIR filtering are realized separately. In recent work, the DAFIC concept has shown significant advantages for the implementation of adaptive transversal structures required in baseband digital transmission applications with echo cancellation.

REFERENCES