Quasi-Second Order \( \Sigma \Delta \) Modulator
Based on Phase-Integration

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Abstract

A sigma delta modulator incorporating a linear phase integrator instead of a conventional voltage-domain integrator is described. The architecture allows achieving a quasi-second order noise shaping by using a passive SC low-pass filter in the first stage. Simulation results demonstrate that the circuit can operate with sampling frequencies of hundred of MHz while obtaining a figure of merit (FoM) well ahead of the state-of-the-art.

I. INTRODUCTION

The use of the sigma-delta technique is more and more common because it allows using digital technologies and relaxes the requirements of the analog blocks used. The technique, initially used to achieve a high number of bits in the audio band, is now employed for communication needs. Many applications require medium resolution with wide signal bandwidth and, very relevant, it is necessary ensuring very low power consumption. Recent research efforts move in two directions: to use sampled-data schemes that need OTAs with a suitable bandwidth and slew-rate, and utilizing continuous-time architectures that allow using g_m-C integrators for exploiting a good power-linearity trade-off. In both cases, when the signal band is in the MHz or ten of MHz range, the oversampling ratio (OSR) can not be too high because at many hundred of MHz OTAs or transconductors are not able to provide the required gain and slew-rate.

Consider, for instance, a signal band of 2 MHz and an OSR = 64. If the number of bit of the quantizer is 1.5 (3 levels) a DR = 77 dB and a peak SNR around 71 dB are expected, features that well meet the requests of several telecommunication applications. However, the sampling frequency is as high as 256 MHz and the expected OTA unity gain frequency must be in the 500 - 800 MHz range. Moreover, with 1 \( V_{pp} \) signals, the slew-rate should be 1 V/ns or so. With 0.5 pF sampling capacitor, the current needed by an OTA able to provide the given slew-rate is typically 0.5 - 1 mA, leading to a power consumption of nW. Summing up, the power required by the entire modulator can be, with signal band of few MHz, several mW with a corresponding figure of merit (FoM) of 0.5 - 1 pJ/conv-level.

The above estimations correspond to state-of-the-art results and are the reference for assessing performance of the modulator presented in this paper, whose design goal is to halve the state of the art FoM and using a minimum silicon area. The transistor level simulations of the proposed modulator obtain a peak SNR of 59.8 dB, the estimated power consumption is 0.5 mW with a FoM of about 0.2 pJ/conv-level.

II. CIRCUIT DESCRIPTION

Recent publications [1], [2], propose to use, instead of an integrator in the voltage domain, an integrator in the phase domain (or time domain), by transforming the input signal into a time information by a voltage-controlled oscillator (VCO). A critical issue in these VCO-based modulators concerns the linearity of the voltage-to-frequency response. The VCO scheme used in the proposed modulator is shown in Fig. 1. It consists in a linear V-to-I converter made by the transistor \( N_2 \) and the resistor \( R \). The current \( I_{N_2} \), flowing trough \( N_2 \), discharges the capacitor \( C \) with a constant slope. When the threshold of \( P_2 (V_{P2}) \) is crossed, the two inverters drive \( P_1 - N_1 \) that recharges \( C \). Therefore, the period of the oscillator is

\[
T_{out} = \frac{RC(V_{dd} - |V_{P2}|)}{V_{IN} - V_{N2}} + \Delta T
\]

where \( V_{N2} \) is the threshold of \( N_2 \) and \( \Delta T \) is the delay of the inverters and the “nand” gate. If \( \Delta T \) is negligible, the period is inversely proportional to the fraction of the input voltage that exceeds \( V_{N2} \).

Fig. 1 – Schematic and symbol of the phase integrator.
Fig. 2 shows the block diagram of a first order $\Sigma\Delta$ modulator based on the phase integrator of Fig. 1. Suppose measuring $T_{\text{out}}$ by using a reference period $T_{R}$. If in $M$ reference periods there are $k$ $T_{\text{out}}$ periods, it results

$$\frac{k}{M} = \frac{V_{\text{IN}} - V_{\text{ref}}}{V_{\text{ref}} - V_{\text{IN}}}$$

(2)

equivalent to the conversion of $V_{\text{IN}}$ obtained by a ramp converter. Moreover, with a simple logic it is possible to measure the number of output pulses in the reference interval. The result is that the output signal is the sigma-delta bit stream of a first-order modulator. Obviously, if $T_{R}$ is much longer than $T_{\text{out}}$ many pulses are measured, thus leading to a multi-bit output.

As known, a first order architecture is not a convenient solution since, with a small number of bits, the spectrum of the shaped quantization error contains tones that fall in the signal band, causing a poor SFDR [3]. Unfortunately, the extension of VCO based schemes to higher order is not easy because, like for architecture of Fig. 2, a VCO provides only the digital output and cannot be used as equivalent of an analog integrator.

The quasi-second order scheme proposed here is based on the transformations depicted in Fig. 3, starting from conventional second order architecture. Fig. 3(b) is the equivalent of the second order architecture of Fig. 3(a) with a phase-$\Sigma\Delta$ (notice that the scheme outlines the quantization error to emphasize the fact that the output is “digital”). Observe that the phase-$\Sigma\Delta$ embeds the local feedback made by the second sum. Fig. 3(c) introduces a loss, i.e. $(1-\alpha)$, in the first integrator and a possible gain factor $k$. The loss moves the pole from $z = 1$ inside the unity circle and affects the NTF at low frequency. In Fig. 3(d) the gain factor $k/(1-\alpha)$ is moved inside the phase-$\Sigma\Delta$ leaving in the first block the transfer function of a passive SC whose implementation, including subtraction, can be realized by the circuit diagram of Fig. 4.

Notice that the gain included in the phase-$\Sigma\Delta$ can be easily implemented: the gain of the phase integrator of Fig. 1 depends on the discharge current and on the value of the capacitor. Therefore, the gain is simply controlled by changing the RC product.

Note that the result is not a second order $\Sigma\Delta$ modulator because the first integrator is with loss and, for this reason, it is here referred to as quasi-second order architecture. The benefit is that the first stage is realized by a passive scheme that requires minimum power. The increased gain of the phase integrator does not increase the power consumption that mainly depends on the value of C and the digital functions used in the scheme.
Since it is important to estimate the possible performance degradation when transforming a second order scheme into a quasi-second order equivalent, extensive behavioral simulations have been performed with different values of $\alpha$ and global gain $A_0 = k/(1-\alpha)$. The obtained results are summarized in Fig. 5, 6 and 7. They correspond to an OSR = 64 and 1.5-bit quantization. Under these conditions, a conventional second order modulator gives a peak SNR = 71 dB. The quasi-second order modulator with $\alpha = 0.94$ and suitable values of $A_0$ obtains a peak SNR (Fig. 5) close to 68 dB and it drops down when $A_0$ becomes too high (> 12).

Fig. 6 plots the peak SNR for different values of $\alpha$ as a function of the global gain. There is an optimum value and a slight reduction in a good range of variation. When the gain is too low the peak SNR drops significantly.

Fig. 7 shows the detail of the output spectra for different values of $A_0$. The shaping at high frequency has a 40 dB per decade slope while at low frequency the slope drops at 20 dB per decade because of the ineffectiveness of the loss integrator in that frequency range.

The results correspond to what predicted by the analysis in the z-domain of the circuit of Fig. 3(c), that yields

$$\text{OUT} = \frac{\text{IN} \left( k z^{-2} \right) + \epsilon_0 \left( 1 - z^{-1} \right) \left( 1 - \alpha z^{-1} \right)}{1 - \left( 1 - \alpha \right) z^{-1} + \left( \alpha + k \right) z^{-2}}$$

It can be noted from (3) that, at low frequencies, the noise transfer function can be approximated by $(1-z^{-1})/A_0$.

III. IMPLEMENTATION ISSUES

One possible goal is using very high sampling frequency. As a matter of facts, the scheme of Fig. 1 reaches many hundred of MHz with power consumptions of ten of $\mu$W. Therefore, large signal bands together with large OSR (like 32, 64 or more) are possible. The reference period can be generated either by a second PI block, as shown in Fig. 2, or, possibly, by an external clock. The first solution is preferable as it allows a good control of the full-scale amplitude.

As shown in Fig. 2, the number of signal pulses gives the output bit stream during the period of the reference signal. A simple circuit that achieves the function $(1-0)$ consists in a SR-FF followed by a D-FF (Fig. 8). A combination of the same circuit is used for multi-bit.

Fig. 5 – SNR versus the input amplitude with $\alpha = 0.94$ and different values of $A_0 = k/(1-\alpha)$.

Fig. 6 – SNR versus the global gain $A_0$ with different $\alpha$.

Fig. 7 – Output spectrum with three values of $A_0$ and $\alpha = 0.94$.

Fig. 8 – Pulses detector.
The solution of Fig. 8 is suitable for low frequencies; however, when the SET and RESET controls (i.e., the pulses $T_{IN}$ and $T_R$, respectively) are almost coincident, there is the risk of malfunctioning that possibly gives rise to the loss of output pulses or a loss of reset. The resulting error is disruptive if the number of wrong pulses is more than a fraction of $\%$ of the total. Indeed, a possible missing or extra pulse gives rise to a white noise, with power equal to the one of the pulse itself, uniformly spread over the entire Nyquist interval. The limit is negligible if the length of the pulses (around $\Delta T$) is very small with respect to the period, as the probability to have an error is very low. However, since $\Delta T$ is hundred of ps, at sampling frequencies in the hundred of MHz range the problem becomes significant.

The request of avoiding any loss of pulses is fulfilled by a double pulse detection technique that uses two strobe signals with a proper delay, as shown in Fig. 9. The second detector picks up the pulses that fall in the gray time interval during which the SR-FF is in the reset phase. The reset is also delayed after the strobe to ensure a proper operation of the D-FF. If a pulse falls in the gray period, it is recovered and assigned to the successive time slot. The timing assignment is not problematic because, if causing an error, it is limited to moving the pulse, say $P(KT)$ from the time slot $(n+1)T$ to nT. This corresponds to adding $P(nT) - P(nT+T)$ to the input bit stream, which effect is equivalent to a unity pulse passed through the high-pass transfer function $(1 - z^{-1})$.

IV. SIMULATION RESULTS

The proposed quasi-second order $\Sigma\Delta$ modulator has been designed and simulated at the transistor level using a conventional 0.18-μm CMOS technology. When the sampling frequency becomes very high, then the delay $\Delta T$ caused by the inverters of the scheme of Fig. 1 is no more negligible and its effect must be accounted for. Equation (2) becomes

$$\frac{k}{M} = \frac{V_{IN}}{y + V_{REF} \Delta T}; \quad y = RC(V_{DD} - V_P)$$

where $V_{IN}$ and $V_{REF}$ use $V_{QU}$ as reference.

Notice that low-pass filter and the possible decimation after the modulator extracts the normalized value of k from the noisy output bit stream. Therefore, the result is not the input but its non-linear processing by the function $y = x/(1 + \beta x)$, $\beta = \Delta T/y$. Accordingly, it would be necessary to compensate for the effect described by (4). One solution is to cancel out the caused distortion in the digital domain. The operation is possible if the parameter $\beta$ is properly estimated at the start up or with an off-line calibration phase.

The limit caused by the finite extra delay $\Delta T$ brings about even and odd harmonics. If the specifications are not very demanding, it is possible to obtain acceptable results by eliminating only the even harmonics using a fully differential approach. Both solutions (i.e., linearization in the digital domain and fully differential approach) to the limit caused by the finite extra delay $\Delta T$ have been implemented. The simulations at the transistor level show that with digital linearization the obtained SNR is just 3 dB below the equivalent behavioral simulations (Simulink™) (peak SNR = 59.8 dB) while the use of a fully differential structure yields 56.6 dB with a third harmonic tone at -59 dB$\nu$. Therefore, the simple fully differential solution looses (3.2+3) dB with respect to the result of the more complicated digital linearization.

Fig. 10 shows the simulated differential output spectrum of the modulator. This result has been obtained by using $\alpha = 0.94$ and $A_0 = 7$. The sampling frequency is 256 MHz, the signal band is 2 MHz. The signal is -6 dB$\nu$ and the power supply is 1.2 V.

The power consumption performances are very attractive: the PI block (Fig. 1) with $C = 35 \, \mu F$ dissipates 52 $\mu W$ and the scheme of Fig. 9 consumes 34 $\mu W$ when running at 256 MHz. A rough estimation of the power of the entire modulator leads to less than 0.5 mW. Accordingly the FoM is about 0.2 pJ/conv-$\nu$.

REFERENCES

