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Design of an Ultra-Low Power
Time Interleaved SAR Converter

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Abstract — An ultra low-power SAR ADC is presented. The circuit is the interleaved version of an already designed SAR converter with improved performance. This design uses 7 interleaved converters and achieves a conversion rate of 700 kS/s. The converter has been simulated by using a 0.18-µm CMOS technology showing a power consumption as low as 40 µW which allows obtaining a state-of-the-art FoM equal to 37 fJ/conv.-step. The architectural study together with converter simulation results are presented.

I. INTRODUCTION

The power consumption is important for micro-sensors wireless systems. After performing a first analog processing, many architectures use an A/D to move into the digital domain. The typical requirements for many sensor systems are medium resolution (~10–12 bit) and low speed (~500-700 kS/s). Therefore, the specs are not difficult but the required low power level is very challenging. Among the data converter architectures, the flash is a first generic option: it uses \((2^n-1)\) comparators. However, the high number of comparators makes the architecture too power hungry even for low resolutions. Also the pipeline architecture is not a good approach for ultra low-power. As known, a pipeline converter reduces the power as it divides the conversion task into several consecutive steps; however, each stage uses an active gain element whose power equals the one of many comparators. Therefore, it becomes competitive for high resolution and, in general, requires too much power. Other architectures, like the sigma-delta and the time interleaved have similar limits because despite their use of speed or multiple paths to increase resolution or throughput, they use active power hungry elements. If the speed is low the most suitable algorithm is the successive approximation that uses a successive approximation register (SAR) to control a DAC in a feedback loop with a single comparator. The cost is that it requires \(n+1\) comparison cycles to achieve \(n\)-bit resolution. The above considerations are summarized in Fig. 1, that shows the best data converter topologies as a function of the desired sampling rate and the required output bit resolution. The diagram depends on the technology and the used supply voltage; however, the SAR algorithm is preferable for signal bands up to one, two hundred of kHz.

As known, the SAR architecture has a circuit configuration like the one shown in Fig. 2, [1 - 4]. The comparator refers to ground after the subtraction of the sampled-and-held input and its foreseen version generated by the DAC. The given topology increases the resolution by just increasing the number of cycles of the algorithm; therefore the power has the logarithmic dependence with the number of quantization steps.

Starting from this favorable algorithm, this work studies architectural strategies to optimize the power consumption of a medium-speed medium-resolution SAR ADC. Namely, a careful design of a SAR architecture, [5], and the use of the time interleaved technique achieves ultra low power. With a 0.18-µm CMOS technology and a sampling rate of 700 kS/s, the expected power consumption is 40 µW, giving rise to a FoM as low as 37 fJ/conv.-step.
II. SAR CONVERTER BASIC BUILDING BLOCKS

The basic architecture of Fig. 2 has been realized with non-conventional and custom designed circuits to minimize the consumed power. This Section discusses the design strategies and provides circuit details. The foreseen resolution is 12-bit (enough for many sensor systems) with a reference voltage of 1 V and supply voltage $V_{DD} = 1.2$ V.

A. DAC

Fig. 3 shows the circuit schematic of the DAC, the input S&H and subtractor. It consists of two identical 6-bit sub-array binary weighted capacitors with unary attenuation capacitor. The use of two sub-arrays is a common way to reduce the capacitor spread and, consequently the power due to the charging and discharging of capacitors during the conversion cycles. However, as discussed in [1], the capacitor used to bridge the two arrays and ensure the attenuation factor of 32 should be non unity. The solution of Fig. 3 uses a unity capacitor but the sub-array is made by 63 elements instead of 64. This causes a global gain error that is acceptable, [6]. The value of the unity capacitance is at least 100 fF and the power consumption turns out to be about 570 nW.

![Image](binary-capacitors-arrays-attenuation-capacitor.png)

Figure 3. Binary capacitors arrays with attenuation capacitor.

The solution of Fig. 3 is the same used in [5], but the switches used for the input sampling are driven by a clock-boost, shows in Fig. 4. The switch transistor is MN1 and the others allow controlling the switch transistor with the same overdrive despite the input variations. The charge and discharge of bootstrap capacitors in the switches introduce a power consumption of about 850 nW.

![Image](bootstrapping-switch.png)

Figure 4. Schematic of a bootstrapping switch.

B. Time-Domain Comparator

Conventional SAR ADCs foresee the use of a voltage comparator, typically made of a preamplifier followed by a latch stage. Theoretical analysis and simulation results demonstrate that this approach is not the best in terms of power consumption, [6]. In order to minimize the power consumption, in this paper, a power effective time-domain comparator is used. Two identical voltage-to-time (V2T) converters make the core of the time-domain comparator, [5].

The V2T, depicted in Fig. 5, provides an output pulse which is delayed with respect to the reference clock, $\Phi_C$, as a function of the input voltage, $V_i$. This process is based on a voltage-to-current conversion (i.e., the input voltage into the current flowing through $R_D$). This current is used to discharge capacitor $C$ with a constant slope. When voltage $V_C$ crosses the threshold of transistor $M_5$, the output voltage $Out_{V2T}$ rises, driven by a tapered inverter chain.

![Image](V2T-schematic-diagram.png)

Figure 5. V2T schematic diagram.

A simple flip-flop delay (DFF) identifies the faster signal between the two V2T output pulses. The digital logic connected to the gate of transistor $M_2$ has the purpose to stop the discharge of the capacitor $C$ after the commutation of the signal $Out_{V2T}$, as shown in Fig. 6.

![Image](V2T-output-pulse.png)

Figure 6. Voltage across $C$ without and with the digital logic on gate of $M_2$.

In this way the power consumption spent for a comparison step decreases of at least a factor two. The most important limit on the value of capacitance $C$ is the thermal noise which imposes at least 0.8 pF. Therefore, the estimated power related to the comparator is about 880 nW.

When designing a time-domain comparator, the time error, conceptually described in Fig. 7, introduced by the DFF has to be taken into account.
This error can be considered as an equivalent input voltage of

\[ V_{\text{IN,eq,er}} = \frac{t_{ji}}{T} \cdot \left( V_{\text{ref}} - V_{\text{GS5}} \right) < \frac{V_{\text{REF}}}{\sqrt{2} \cdot 2^{n+1}} \]  

(1)

where the time \( t_{ji} \), characteristic of the time comparator, is equal to 130 ps, \( V_{\text{ref}} \) is the input voltage of the V2T used as reference, and \( V_{\text{REF}} = V_{\text{REF+}} - V_{\text{REF-}} \). Therefore, to obtain an equivalent input error less than a quarter of LSB, it is required a comparison time of at least 226 ns.

\[ \text{Figure 7. Considerations on time error.} \]

C. SAR

As mentioned above, to meet the low power requirements, the successive approximation register is full custom designed, which implicates a power consumption of about 1.8 \( \mu \)W. It is worth to point out that the SAR logic generates also the A/D converter control phases. The SAR logic is optimized for minimum power consumption. The conversion requires 14 clock periods of the main clock: the first for the input sampling, 12 periods are for the successive approximation cycles and the last one for end of conversion and data transfer.

III. TIME INTERLEAVED SOLUTION CONSIDERATIONS

The SAR converter requires 14 clock periods to obtain a single conversion and this limited comparison speed of the time-domain comparator motivates the choice to consider a time interleaved approach to meet the required conversion rate. The number of different paths used in this approach must to be equal to an integer divisor of the number of clock periods needed for a conversion with a simple SAR. In particular, in this paper, an architecture with 7 parallel paths is analyzed.

In the single-path solution, as described above, two V2T converters are used in the time-domain comparator, one to process the input signal (signal V2T) and the other used as a reference (reference V2T). This choice ensures good matching performance between the two V2T blocks. When considering a 7 parallel paths solution, it is possible to use only one reference V2T for all 7 signal V2Ts, as shown in Fig. 8. This solution, obviously, allows strongly reducing the power consumption.

When approaching a time interleaved topology, issues related to gain and offset errors have to be carefully analyzed. In a time interleaved SAR ADC, the gain error of each converter depends mainly from the DAC. In this work, the DAC has been designed with analog output as a function of the reference voltages. It has to be pointed out that the reference voltages are the same for all DACs present on each path, thus leading to any gain error. The gain error depends also on DAC capacitors mismatch, but the DAC structure adopted in this design allows obtaining good matching performance, [6].

\[ \text{Figure 8. Time interleaved solution with SAR converter based on time-domain comparator.} \]

The second critical issue to be considered when designing a time interleaved ADC is the offset error. In the case of a time interleaved SAR converter, the block that introduces this kind of error is the comparator. In our design, different sources of V2T input offset are present: mismatch among capacitors \( C \) or resistors \( R_D \), transistor \( M_f \) threshold variations, and FFD time errors. The basic idea in order to compensate for all these offset contributions is to trim the value of resistor \( R_D \) by means of an adequate digital trimming circuit. This leads to reduce the equivalent input offset below half LSB. To estimate the overall equivalent input offset of a reference V2T with comparison time equal to 230 ns, several Montecarlo simulations have been performed. As a result, it has been verified that the comparison time is in the range from 200 ns to 260 ns. Translating these time values in the voltage domain, it means that the possible equivalent input offset can assume values from -43 mV to +40 mV. Considering that half LSB is equal to 122 \( \mu \)V, it is apparent that the digital trimming of resistor \( R_D \) is not effective. The idea is to perform first a coarse offset reduction by trimming on each DAC the bias voltage, referred to as \( V_{\text{bias}} \) in Fig. 3, and then the fine digital trimming of resistor \( R_D \). The manual course calibration precision is typically of about 10-15 mV. With regard to the fine digital trimming design, it is worth to point out that a V2T input offset error equal to half LSB can be compensated for by a \( R_D \) variation of 330 \( \Omega \). In this way, at least 100 330-\( \Omega \) resistors are required to compensate for the residual offset of 10-15 mV. This leads to a digital trimming that foresees the use of 7 bits (i.e., 128 steps).
Considering the technology mismatches on resistors values, a nominal resistor of $312 \, \Omega$ is used. Considering mismatch, this resistor can vary from 294 to 330 $\Omega$ so that an overall input offset of 13.9-15.6 mV, respectively, can be corrected. The power consumption of the digital logic which manages the time interleaved structure is estimated to 10 $\mu$W.

IV. SIMULATION RESULTS

The proposed time interleaved SAR ADC has been realized at the transistor level and simulated by using a conventional 0.18-µm CMOS technology. The used power supply value is 1.2 V. Fig. 9 shows the simulated output spectrum (obtained with 1024 samples) of a SAR converter. The sampling rate is 100 kS/s and the sine wave input signal frequency is 29.8 kHz. It can be noted that the noise floor is almost flat. The simulated SNDR is equal to 65.6 dB.

Fig. 11 shows a behavioral dynamic simulation of the 7 parallel paths time interleaved SAR converter after the digital correction of the offset. The output spectrum depicted in Fig. 11 has been obtained including an offset error with standard deviation equal to 2 LSB. The frequency of the input sine wave is 200.9 kHz. It can be noted that the second and the third harmonics are present. The second harmonic tone, placed at about 300 kHz, is at -78 dB while the third harmonic tone, placed at about 100 kHz, is at -81 dB. The simulated power consumption of the time interleaved SAR ADC is about 40 $\mu$W. This value leads, considering a signal bandwidth of 350 kHz, to a FoM as low as about 37 fJ/conv.-step.

CONCLUSIONS

In this paper, an ultra low-power time interleaved SAR ADC is presented. This design uses 7 interleaved converters and achieves a conversion rate of 700 kS/s. Design considerations about time-domain comparator offset calibration have been drawn. The A/D converter has been simulated at the transistor level by using a 0.18-µm CMOS technology. The simulated power consumption is as low as 40 $\mu$W which allows obtaining a state-of-the-art FoM equal to 37 fJ/conv.-step.

REFERENCES