VLSI IMPLEMENTATION OF THE METERING SIGNAL GENERATOR FOR SWITCHING SYSTEM ANALOG TERMINATIONS

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Abstract

In this document we will briefly describe a mixed analog–digital integrated circuit to be employed in a Central Exchange Switching System. This generates a proper shaped telephone metering pulse, according to the actual international standards, and sends it to eight subscribers. It has been designed with a cell–based approach and implemented with a 3 μm double poly single metal CMOS technology. The 80% of the circuit uses digital and analog cells, while 20% has been specifically designed down to a transistor level. In order to reduce the power consumption two different supplies was used.

INTRODUCTION

Modern electronic Switching System requires more reliable and cost effective circuit solutions. These aims may be achieved by adopting very large scale integration and semi–custom circuits.

The most recursive block in a local switching system is presently the analog subscriber interface; therefore much effort is spent here to obtain cost effective, more integrated solutions and low power consumption.

One of the functions included in the analog subscriber interface is the metering signal injection; the metering signal is a shaped sinusoid (Fig. 1), which may have a frequency of 12 kHz or 16 kHz.

The role of this signal is to activate a "metering counter" sited at the subscriber premises so it must satisfy some specific requirements, as regards the amplitude and the total distortion.

This communication describes a 3 μm CMOS integrated circuit which generates the metering signal for 8 subscriber interfaces, suitable for both the 12 kHz and 16 kHz standard, and capable of driving a load of 5 kOhm, with an amplitude of 1 Vp at each output.

1. SYSTEM DESCRIPTION

The block diagram of the integrated circuit is shown in fig. 2.

Fig. 1 – Example of amplitude envelope.

Fig. 2 – Block diagram.
The circuit generates and shapes a sinusoidal signal whose frequency can be set to 12 kHz or 16 kHz by an external pin (PREF). Shaped sine signals are sent to the 8 outputs by a proper command interface. The used main clock is 2.048 MHz.

The sinusoidal generator, described in details in the next sections, generates a 16 levels sine signal when driven by proper digital phases.

The modulator needs specific phases too; all of them are generated in the digital phases generator block.

The digital input interface is a switching matrix capable to combine a rising modulated signal, a flat sinewave or a falling modulated signal and to send the result to the proper output.

2. SINUSOIDAL GENERATOR

The sinusoidal generator is the core of this circuit. It consists of:

- a step waveform generator;
- a switched capacitors filter;
- a continuous time filter;

During phase $PA_0$ the output is grounded; at the same time the operational amplifier is connected in the buffer configuration making available the operational amplifier offset $V_{os}$ at the virtual ground terminal. This makes it possible to precharge the capacitors $C_1 - C_4$ to $V_{ref} - V_{os}$ and to discharge $C_5$ to $V_{os}$. During the successive phases the capacitors $C_1$, $C_2$, $C_3$, $C_4$ inject sequentially their charge into $C_5$. The values of $C_1 - C_4$ are such that samples of the first half period of a sine wave is generated. The second half period is got by the same circuit in the non-inverting configuration. The initial precharging of the injecting array to $V_{os}$ makes the operation of the circuit insensitive to the operational amplifier offset.

The 16 kHz frequency is created by using a clock interval $T_i$ equal to 8 periods of the master clock (2.048 MHz). The generation of the 12 kHz frequency is more complex, since it may not be obtained by a simple division of the master clock. It has been verified that a negligible harmonic distortion is introduced if a small jitter appears in the clock intervals $T_i$. This allows to solve the problem of generating the 12 kHz by simply generating successive $T_i$ periods as sequence 11 - 11 - 10 clock master period.

The sinusoidal generator has been simulated with the mixed mode simulator SABER [2] using AMS library components [3]. The output waveform is shown in fig. 5.
Fig. 5.6 – Output of the step generator (measured).

It should be noted that the generator output contains wide spikes. They are due to the clock feedthrough effect. However, they are not a serious problem since they introduce high frequency components that are filtered out by the following blocks. The sinusoidal generator is cascaded with a conventional biquad low pass switched capacitors filter [4] and a continuous time smoothing filter. The used configuration is a Sallen and Key structure with nominal cut off frequency equal to 83 kHz.

3. WAVEFORM GENERATOR

The waveform shown in figure 1 is generated by a proper selection of one of the three waveform signals shown in figure 6.

Fig. 6 – Output signals from the modulator.

The first waveform corresponds to the rising section, the second one is a pure sine wave and is suitable to generate the flat section while the third waveform corresponds to the falling section.

The required waveforms are generated by two 4 bits MDAC whose reference voltage is the generated sinewave. The two DACs share the same resistor string. In order to spare silicon area the command to the step switches are synchronized with the zero crossings of the sinusoidal signal.

4. DIGITAL PART

The digital section of the circuit can be divided into two blocks, the command interface and the timing block.

The first one latches and synchronizes the external commands with the beginning of each 16 ms rising and falling period. Moreover, it addresses the outputs of the waveform modulator to the proper output for the foreseen time slots.

The timing block generates the clock phases required by the sinusoidal generator and the waveform modulator by a proper division of the master clock.
5. CONCLUSION

The circuit has been integrated in a 3μm CMOS double poly single metal technology. The design methodology is standard cell for the digital section (80% of the chip area) and full custom for the analog section.

The die size, including pads, is 3.5 x 3.8 mm², the microphotograph is shown in fig. 7.

The used package is 20 pins DIL.

References


Fig. 7 – Chip microphotograph.

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