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Third-Order $\Sigma \Delta$ Modulator with 61-dB SNR and 6-MHz Bandwidth Consuming 6 mW

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Abstract—This low-power sigma-delta modulator targets the DVB-H requirements and achieves about 10 bit with 6-MHz signal band and a FoM of 0.59 pJ/conversion. The used scheme is a multi-bit third order modulator that, with suitable topological modification, enables using two op-amps and enjoying a swing reduction at the quantizer input. The area of the circuit, fabricated with a 0.18-μm analog CMOS technology, is 0.32 m². The nominal supply voltage is 1.8 V and the clock frequency is 96 MHz (OSR = 8). Experimental measurements confirm the behavioral study made accounting for the op-amps limitations.

I. INTRODUCTION

Sigma-delta modulators are more and more used for portable telecom applications. Well-known advantages are: minimum requests of analog accuracy, good figure of merit (FoM) and medium-high resolution with a relatively low oversampling ratio (OSR). According to this trend it is expected that the challenging band (4-8 MHz) and power consumption (less than 10 mW) requirements for digital video broadcast for handhelds (DVB-H), [1], can be satisfied with power optimized $\Sigma \Delta$ solutions.

This paper uses a third order $\Sigma \Delta$ architecture with a 5-bit quantizer, [2]. Therefore, if the expected resolution is 10 bit, an OSR as low as 8 can be used, as it grants an extra 42-dB SNR. The circuit does not use any DEM because the expected linearity of the resistor-based DACs is sufficient. The key characteristics of the circuit to reduce the power consumption is the use of only two op-amps, [3], and just 18 voltage comparators instead of 31 in the flash while ensuring an overall 5-bit accuracy.

The proposed third-order sigma-delta modulator has been integrated by using a 0.18-μm analog CMOS technology. Experimental results show 9.8 bit of accuracy at 96-MHz clock (6-MHz signal bandwidth). The resolution slightly increases at lower clock and equal SNR because of the reduced spur noise injected by the DAC, especially the one on the second stage. The total power consumption is as low as 6.18 mW with 1.8-V supply voltage, resulting in a remarkable FoM of 0.59 pJ/conversion.

II. LOW POWER STRATEGIES

In order to reduce the power consumption it is necessary to identify power hungry components and to limit their power request and, possibly, their number. Since the power of an op-amp increases in a quadratic way with its bandwidth, it is mandatory to keep at the minimum the clock frequency and, accordingly, the OSR. However, with low OSR, it is necessary to use high-order modulators, that means more op-amps, or to augment the resolution in the quantizer, that means more comparators. The trade-off depends on the power required by the single blocks. For this reason, we made preliminary transistor level simulations with the used technology. We obtained that an op-amp with 600-MHz bandwidth, 300-V/μs slew-rate, and 60 dB of gain consumes 2.3 mW, and a comparator with 5-mV sensitivity clocked at 100 MHz consumes about 60 μW. The numerical result provides the architecture recommendation: use the maximum number of bit in the quantizer and the lowest OSR.

A. Reduction of the number of op-amps.

Fig. 1 shows the chosen basic sigma-delta scheme, [2]. It is a third order modulator with a cascade of three integrators without delay. The coefficients that makes the noise transfer function (NTF) equal to $(1 – z^{-1})^3$ are shown in the diagram.

Fig. 1 – Third order sigma-delta modulator with 5-bit quantizer.
Since a large output swing of an op-amp demands for high slew-rate, it is worth using a feed-forward path, as shown in Fig. 1, that limits the swing of the first op-amp to almost the quantization noise.

![Diagram of Fig. 1](image1)

The reduction of the swing at the input of the flash determines two benefits: the slew-rate of the second op-amp is relaxed and the number of comparators decreases from 31 to 18 for 5-bit quantization.

The cost that must be paid is due to the coefficient 3 in the block diagram depicted in Fig. 5 that imposes a non favorable feedback factor. This requires a more demanding bandwidth and slew-rate in the op-amp. The problem can be possibly limited by using an attenuation factor in the Double Integrator block that is compensated for with a corresponding reduction in the flash quantization interval. The possible need of a higher gain in the comparators is likely demanding a smaller increase of power than the one likely demanding a smaller increase of power than the one.

![Diagram of Fig. 5](image5)

### B. Reduction of the number of comparators.

The power required by the quantizer is mainly due to the flash. Indeed, the power of the DAC is negligible because it is mainly given by the generator of the quantized voltages. The technique used to reduce the number of comparators in the flash starts by observing that for many bit and a given OSR, there is a good correlation between two successive flash inputs. Therefore, it is more convenient to quantize \((V_{QD}(n) - V_{QD}(n - 1))\) than \(V_{QD}(n)\). This leads to the scheme of Fig. 3, which, indeed, foresees the quantization of \((V_{QD}(n) - V_{QD}(n - 1))\), where \(V_{QD}(n - 1)\) is the result of the previous quantization. The \(z^{-2}\) term after the quantizer represents a full clock delay. However, in the real implementation it is divided in two half delays, one used in the flash and the other in the previous block in the modulator.

![Diagram of Fig. 3](image3)

The use of the scheme of Fig. 3 into the modulator gives the diagram of Fig. 4. Since the subtraction at the input of the quantizer would require an additional active block, that branch is moved back multiplied by \((1 - z^{-2})\). The result is that the feedback signal at the input of the block referred to as Double Integrator becomes

\[
-(2 - z^{-1}) - (1 - z^{-1})^2 = -3(1 - z^{-1}) - z^{-2}
\]

leading to the block diagram of Fig. 5.

![Diagram of Fig. 4](image4)

![Diagram of Fig. 5](image5)
needed by the op-amp. A study of the problem at the transistor level showed an expected but limited benefit so that, to ensure a more robust solution, we opted for the original approach.

III. CIRCUIT IMPLEMENTATION

The two op-amps used to implement blocks Integrator 1 and Double Integrator have the same scheme but use different bias currents as requested by the slew-rate and bandwidth: they are fully-differential folded cascode amplifiers with switched capacitor common mode feedback. The input capacitor in the first integrator is 80 fF and the feedback capacitors in the Double Integrator is 40 fF. The op-amps key features are summarized in Table 1.

<table>
<thead>
<tr>
<th>Feature</th>
<th>First op-amp</th>
<th>Second op-amp</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>1.8 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>580 MHz</td>
<td>890 MHz</td>
</tr>
<tr>
<td>Slew-rate</td>
<td>300 V/μs</td>
<td>400 V/μs</td>
</tr>
<tr>
<td>Gain</td>
<td>51 dB</td>
<td>48 dB</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.9 mW</td>
<td>2.4 mW</td>
</tr>
</tbody>
</table>

A 5-bit DAC made by an array of capacitors would require using 32 unity elements whose value should be too small to ensure the required matching performance. For this reason, the DACs have been realized by using a resistive divider with 32 equal resistances of 200 Ω. Moreover, in order to avoid interferences and reduce the digital processing, the input of the Double Integrator uses two DACs. The used solution implies some additional power consumption, that is, however, about the 15% of the total.

Fig. 6 shows the schematic diagram of the voltage comparators used in the sigma-delta modulator. It is a two-stage fully differential scheme. The first stage (top of the Fig. 6) is a preamplifier with a gain of 9.3 dB and continuous time common mode feedback. The second stage (bottom of Fig. 6) is the regenerative latch. Simulation results show a response time of about 2 ns after the signal clock (Φ) triggering. The bias current of the preamplifier is 25 μA.

IV. MEASUREMENT RESULTS

The proposed third order sigma-delta modulator has been integrated by using a 0.18-μm, double poly, 5 metal levels CMOS technology. The die, whose microphotograph is shown in Fig. 7, has an active area equal to 0.32 μm². The reference voltages are external to the circuit; no internal buffer is used to enforce the strength of the references. To limit the effects of parasitic inductances due to the bonding, a 40-pins LLP package has been used. The nominal supply voltage is 1.8 V.

The proposed modulator has been measured for different sampling frequencies, f_s. At 96-MHz clock, the measured spectrum is given in Fig. 8. Considering an OSR = 8, the signal bandwidth is 6 MHz and the achieved SNDR is 60.7 dB, corresponding to 9.8 bit. The spectrum shows a second and a third harmonic whose amplitudes are -88 and -77 dBFS, respectively. The second harmonic tone is likely due to a small mismatch in the input differential signal.
The measured output spectrum (FFT with 65536 points; dashed line: -60 dB/dec slope).

Fig. 9 compares the measured SNR versus input amplitude for different conditions. The dashed and the solid lines are the ideal and the behavioral simulation results, respectively. For the behavioral study, the used model foresees the real limit caused by the gain, bandwidth and slew-rate of the op-amps given in Table 1, [4]. The experimental data show that when the clock frequency is reduced to 64 MHz and 32 MHz (bandwidth equal to 4 MHz and 2 MHz, respectively), the SNR improves by approximately 3 and 6 dB. The reason of the SNR degradation is ascribed to the noise affecting the DAC signals. Since the circuit does not use internal buffers, the DAC voltage experiences a ringing that settles well within the clock period at $f_s = 32$ MHz, but has some residual for $f_s = 64$ MHz and 96 MHz. Computer simulations show that a white noise injected at the input of the first integrator gives rise to a white spectrum while a white noise injected at the input of the second integrator causes a first order shaped component. This contribution, because of the 3 and the $z^{-2}$ terms and because of the layout of the DACs, is dominant. Its effect is visible in the spectrum of Fig. 8 as it hits the corner of the signal band.

The total measured power with 96-MHz clock is 6.18 mW. Therefore, the achieved FoM is 0.59 pJ/conversion, value that is remarkable if we consider the wide band of the input signal. Table 2 summarizes the performance of the modulator.

<table>
<thead>
<tr>
<th>TABLE II. PERFORMANCE SUMMARY</th>
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</thead>
<tbody>
<tr>
<td>Sampling frequency</td>
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<tr>
<td>Supply voltage</td>
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<tr>
<td>Full scale input signal</td>
</tr>
<tr>
<td>Signal bandwidth</td>
</tr>
<tr>
<td>Peak SNDR</td>
</tr>
<tr>
<td>Active area</td>
</tr>
<tr>
<td>Power consumption</td>
</tr>
<tr>
<td>FoM</td>
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V. CONCLUSIONS

In this paper a low-power third order sigma-delta modulator has been presented. The proposed circuit uses only two op-amps and a reduced number of voltage comparators in the quantizer (18 to achieve 5 bit of resolution). Measurement results show 60.7-dB peak SNDR considering 96-MHz clock and a signal bandwidth of 6 MHz. The total measured power consumption is equal to 6.18 mW. This leads to a FoM of 0.59 pJ/conversion.

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