Design of a 12.5 GS/s 5-bit Folding A/D Converter

Antonio Surano and Franco Maloberti
Department of Electronics
University of Pavia
Via Ferrata, 1 - 27100 Pavia – ITALY
[antoni.surano, franco.maloberti]@unipv.it

Abstract—A 12.5 GS/s 5-bit A/D converter is described. The architecture is a hybrid scheme with flash, single and double folding, able to obtain the optimum trade off between speed and power consumption. Simulations at the transistor level validate the proposed architecture.

Keywords: ADC; Analog to Digital Converter; Folding; High Speed Conversion; GHz.

I. INTRODUCTION

Many modern applications ask for data converters with extremely high conversion speed. The required resolution is typically low (5-bit or less) [1] but the band of signals can be several GHz [2]. Examples are in the area of high-speed data wireline [3] or wireless communication that, with new standards, foresee several Gb/s [4]. The limitation of the transmitting media is compensated for with pre-emphasis before transmission and equalization at the receiver. These operations can be done with analog circuits but are also obtained with digital processing, provided that the transmitted and received signal pass through data converters.

As known, digital processing grants programmability of processing just by changing software. However, there is another important feature: obtaining minimum power consumption and, typically, analog solutions are more power effective than the data conversion plus digital processor. Therefore, the success of digital solution also depends on the consumed power.

The power effectiveness of data converters is measured by the figure of merit:

\[ FOM = \frac{P}{2^{\text{ENOB}}2^B} \]  

(1)

Good values of FoM are below 1 pJ/conv-level. Thus, for \( f_{\text{CK}} = 10 \text{ GHz} \) and \( \text{FoM} = 0.5 \text{ pJ/conv-level} \), the power for level, \( P/2^{\text{ENOB}} \) should be below 5 mW. However, with 5-bit the power consumption would be more than hundred mW, not suitable for many applications. Therefore, it is necessary to develop circuit solutions and architectures that reduce the power consumption significantly.

This paper describes the design of a 5 bit ultra-high speed ADC in nanometer technology. The architecture combines the features of the flash and the folding scheme and consumes 54 mW with nominally 5-bit of resolution.

II. DESIGN STRATEGY

The architecture normally used for high-speed low resolution A/D conversion is the flash. With N-bit it uses \( 2^N-1 \) comparators and some logic that transforms the thermometric code into binary. For low values of \( N \), the scheme of the comparator is very simple because the large quantization step requires a low pre-amplification or no amplification at all. When \( N \) becomes medium the power increases significantly for two reasons: the number of levels augments and the comparators need a substantial pre-amplification.

Solutions that are more power effective than the flash are the two-step flash and the folding. The former is difficult to implement at GS/s because of the need of subtraction and amplification. The latter can be a viable solution if the technology enables very fast folding schemes. Multiple folding reduces the number of bit of the next stage. However, since the folder consumes power there is a trade-off in the choice of the number of folding. Moreover, since folding is not sharp, at the transition points there is a significant non-linearity error. The problem is normally resolved by doubling the folding network with a shift of the folding response. Indeed, for 5-bit duplicating the folding structures is too expensive. A more appropriate solution is to use a flash that converts only the region of non-linearity around the folding points.

In order to find the optimal solution it is necessary to account for the power consumed by each block and to compare the total powers. Fig 1 illustrates the architecture of a plain flash and schemes with single and double folding. The power consumed by each block is outlined in the figure. The power of the sample and hold depends on the driven capacitive load. Since the ratio \( g_m/C_L \) must be kept constant the power of the S&H increases as the square of \( C_L \) that, in turn, is proportional to the square of the number of comparator connected to the S&H. Since the generator of reference voltages must keep constant the charging time constants, its equivalent resistances must decrease with the capacitive load. Therefore, its power is proportional to \( C_L \) and, accordingly, increases linearly with the number of comparators served. The power of a comparator is the sum of the one of the preamplifier and the latch. The gain of the pre-amp depends on the quantization step and increases with the overall resolution. The power of the folder is assumed proportional to the number of folding branches.

Simulations at the transistor level give the values of the power consumption of the blocks with 12.5 GHz clock. The simulations also verify the assumed dependence of power with the capacitive load. The use of obtained values with the three architectures of Fig 1 leads to the following estimated consumed power: flash 135 mW, single folding 80 mW and...
double folding 62 mW. Therefore, the architecture of Fig 1(c) is the optimal and used in this design.

Figure 1. High-speed low resolution A/D, (a) Flash, (b) Single Folding, (c) Double Folding.

III. FOLDING ARCHITECTURE

A. First Folding Circuit

The use of a double folding scheme relies on a first folding circuit that obtains a good linearity in a wide range of the expected dynamic range. The first folder is shown in Fig 2. When the two inputs are equal, the value of V_{REF} determines the pair unbalance and the resulting output voltages. When one of input reaches V_{REF} the differential pair is balanced and the differential output is zero. The circuit included a positive feedback on the load side to obtain gain. Possible static mismatches alter the nominal folded response shown in Fig 3. We have three possible errors, common mode shifts, shown in Fig 3(a) and 3(b) and differential tilt as shown in Fig 3(c). The scheme of Fig 2 enables the correction of the errors by using two folding scheme that work in parallel with different transistor ratio. The trimming of the two bias currents and their common mode value adjust the above mentioned errors.

Figure 2. First folding circuit schematic.

The asymmetry of the circuit makes one output faster than the other. The different delay in the positive and negative responses is corrected with a capacitor load on V_{OUT+}.

Figure 3. Result of (a) (b) common mode calibration, (c) differential calibration.

B. Second Folding Circuit

The second folding circuit is less demanding and can be, for reducing power single ended. Fig 4 shows its circuit scheme. The circuit need a differential input. It is made by two p-channel branches with cross couple input control. If the two inputs are such that the one is low and the other is high then the two paths which connect these transistors are high resistance mode and hence the output is low. With zero differential input, the output is determined by the voltage divider made by the p-channel and the n-channel devices.

Trimming the gate voltage (common mode and differential) of M_{T1} and M_{T2} obtains calibration.
The current sources $M_{T1}$ and $M_{T2}$ control the output response. The common mode value changes the amplification factor (Fig 5(a)), a differential term compensates for possible mismatches (Fig 5(b)).

It is possible to use two calibration signals: a common mode signal and a differential signal. Fig. 7 gives an idea of the range of control.

The track and hold and gain stage use the scheme of figure 6. It is a differential pair with a degeneration resistor and a degeneration capacitor for setting the gain and bandwidth. The differential pair, is made by two pair of elements working in parallel. The used arrangement is for having the same degeneration RC in both sections. A suitable control of the common mode current and the differential term controls of the $I_{BIAS}$ provides the offset voltage compensation. For example, with $N=3$, a differential current variation equal to $\Delta$ produces a current control ranging from $I(1+\Delta)$ to $I(1-\Delta)$ with $\Delta=0.1$, $I=1$ mA.

The architecture uses comparators with single ended and differential input. The used scheme are depicted in Fig 8 and Fig 9. Both comparator use two regenerative loops (p-type and n-type). The output is squared by a S-R latch.

The basic blocks described in the previous section have been used in the architecture of Fig 1(c), it provides three digital signals: the conversion of the input, and the ones of the two folded signals. Since many applications require for a minimum resolution the number of comparator made available by the power budget can be used in a different way with respect to a conventional manner.
Fig 11 describes the used approach. 7 comparators realize a 3 bit flash of the sampled input. In this way the 3-bit resolution is guaranteed. The response with single folding determines the 4-th bit, with 4 comparators being the threshold places in between the MSB levels. The response of the double folding provides the LSB. The total number of comparators is 15 with a resolution of a factor 2 with respect to the full-flash.

**Fig. 11. Threshold levels of the comparators.**

VII. SIMULATION RESULTS

The proposed architecture has been simulated at the transistor levels with a 45nm CMOS technology. Each block has been optimized to achieve the expected speed at the minimum consumed power. The capacitive load of the metal interconnections has been accounted for with parasitic capacitances in critical nodes of the circuit. The value corresponds to the one of the expected metal interconnections.

Fig. 12 shows the time domain response of the Track and Hold with a full scale input sine-wave at 1 GHz.

The time domain response of the Track and Hold with a full scale input sine-wave at 6 GHz is shown in Fig 13.

**Fig. 13. Transient response of Track and hold with a sine-wave input signal at 1 GHz.**

**Fig. 13. Transient response of Track and hold with a sine-wave input signal at 6 GHz.**

Fig. 14 shows the output spectrum of the entire converter, with a sine-wave input at 6.2225 GHz the obtained equivalent number of bit is 4.4.

The simulated power consumption is 53mW at 1 V supply voltage. It not include the power of the digital processing and the clock generator.

**Fig. 14. Output Spectrum of the A/D converter.**

ACKNOWLEDGMENT

The authors would like to thank FIRB, Italian National Program #RBAP06L4S5 and Texas Instruments, Northampton (UK) for partial economical support.

REFERENCES