Smart Dynamic Element Matching for Multi-bit Incremental Modulators

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Abstract A new dynamic element matching technique suitable for multi-bit incremental A/D converters is proposed. The method almost completely compensates for the unity element mismatch in a second order incremental scheme, thus enabling very high resolution with relatively low orders and low-power.

I. INTRODUCTION

Incremental converters are architectures suitable for high-resolution and low-bandwidth A/D conversion. An incremental converter has the same scheme of a sigma-delta modulator but it uses a sampled and held input for the entire conversion cycle. Moreover, the method needs an initial reset of all the integrators. Cascading multiple sampled-data integrators obtains successive accumulation of the input voltage that is amplified by an increasing power of the number of conversion periods, n. A single integrator generates a staircase and amplifies the input by the first power of n. A double integrator produces a parabola and obtains an increase of input by n(n-1)/2, proportional to n^2, a third order obtains an increase proportional to n^3 and so forth.

Since the amplification factor, G, corresponds to the number of quantization levels, the resulting number of bit is log_2G. Therefore, high resolution requires a large number of conversion periods and/or high order modulators. However, to ensure stability third or higher order architectures use methods that attenuate the value of G. A typical reduction for a third order gain is 32.

A single-bit quantizer ensures intrinsic linearity. This is common in incremental schemes because multi-bit solutions would cause non-linearity that are not fixed by the dynamic element error (DEM) techniques, normally used in sigma-delta modulators. That is a misfortune, because multi-bit solutions would grant a substantial reduction of the conversion time. For example, a 3-bit second order modulator achieves 18-bit with only 256 clock periods instead than 724. Obtaining 20-bit needs just 512 clock period instead than 1448.

The above perspective motivates this paper that proposes and verifies at simulation level a smart dynamic element-matching scheme (S-DEM) that is capable to compensate for the mismatches in the capacitive DAC of the incremental scheme, whose unity elements match the kT/C limit. Extensive simulations show that the method obtains an almost perfect correction of mismatch errors.

II. EFFECTIVE INCREMENTAL CONVERTERS

The figure of merit (FoM), defined as power divided by the product 2^{ENB}·f_{conv} (ENB is the equivalent number of bit), serves to assess power effectiveness of data converters. For high-resolution ADC low FoMs indicate precise processing at high bandwidth with good power consumption as needed by portable applications.

Since the double ramp (DR) converter needs 2^{N+1} clock periods to secure N-bit, a clock frequency f_{CK} obtains f_{conv} = f_{CK}/2^{N+1}. Supposing that P_{Ax}, power of the op-amp running at f_{CK}, is the main source of power consumption, it results

\[ FoM_{DR} = P_{Ax} \cdot \frac{f_{CK}}{2^{ENB} \cdot 2 \cdot f_{CK} \cdot 2^{N+1}} = F_N \cdot 2^{N+1} \] (1)

defining the parameter F_N.

A first order incremental scheme needs only 2^N clock periods. Its FoM is half the DR architecture. A second order converter uses two op-amp but needs about 2^{(N-1)/2} clock periods. Therefore, the FoM2 is
$2^{(N+1)/2}$ lower than the one of the DR scheme. The third order modulator needs $n=(3!\cdot32\cdot2^N)^{1/3}$. Therefore, since the scheme uses three op-amps, the reduction of FoM$_3$ with respect to FoM$_{DR}$ is $14.7/2^{2N/3}$. Notice that the gain reduction by 32 in the third order scheme, like the one of Fig. 1 [1], [2], makes FoM$_3$ better than FoM$_2$ for more than 16-bit (with $F_N$ constant). The benefit only doubles at 22-bit.

The use of MASH, popular in $\Sigma\Delta$ schemes, is an alternative solution. It is studied in [3] for single-bit stages (Fig. 2). The architecture does not suffer any reduction of $G$ but requires calibration for correcting the inter-stage gain mismatch.

In summary, single-bit incremental converters with order higher than 2 are problematic and not fully beneficial when the resolution is in the 18-20 bit range.

### III. THERMAL NOISE CONSTRAINT

Noise is a key limit in high-resolution converters. Namely, the switching of the sampling capacitor causes $2kT/C_n$ noise. The first integrator of a second order incremental modulator stores the noise power injected during the first clock period for the entire conversion cycle. Therefore, the second integrator amplifies it by $(n-1)$ times. The next noise sample is accumulated (n-2) times and so forth. Thus, since the noise samples are equal and uncorrelated, at the end of the conversion $2kT/C_{in}$ is amplified by

$$K(n) = \sum_{j=0}^{n-1} j^2 = \frac{(n-2)^3}{3} + \frac{(n-2)^2}{2} + \frac{(n-2)}{6}$$

that, referred to input, is divided by $A^2=[n(n-1)/2]^2$

$$V_{in}^2 = 8kT \sum_{j=0}^{n-1} j^2 = \frac{8kT}{C_{in}} \frac{(n-2)^3}{3} + \frac{(n-2)^2}{2} + \frac{(n-2)}{6}$$

For a given $V_{REF}$ and $N_{in}$ the quantization noise must be at least twice the $kT/C$ contribution given by (2). Therefore, the minimum input capacitance for 1V and 2V $V_{REF}$ must be the value of Fig. 3. Namely, for 20-bit the input capacitance must be as large as 98 pF for $1V_{FS}$ and 24.5 pF for $2V_{FS}$.

![Graph showing the required capacity for given accuracy](image)

Notice that the relatively large input capacitance would enable to split $C_n$ into 8 unity elements with good matching. A typical technology has 1 fF/μm$^2$ specific capacitance and matching accuracy of 0.3%/WL$^{1/2}$. A 12.25 pF is a square of 110.6μm x 110.6μm, yielding 27ppm matching, a value that ensures about 15.5 bit. The accuracy is good but not
enough for very high resolutions.
Since a multi-bit solution reduces the number of clock periods the value of $K(n)$ is lower and the required input capacitance diminishes. Thus, its value depends on the $kT/C$ limit and the matching requirement that result from the DEM method used.

VI. SMART MATCHING METHOD

The error mismatch between unity elements causes a deterministic but unknown injection of errors at the input of the incremental modulator. The processing of these errors is similar to the one already discussed for the noise but their superposition is linear.

Therefore, the error injected at the first clock is, at the end of the conversion, multiplied by $(n-1)$, an error entering at the second clock will be multiplied by $(n-2)$, and so forth. If the same capacitor $j$ is used at clock periods $n_1$, $n_2$, ..., $n_k$, the effect of its error, $e_j$, at the end of the conversion cycle is amplified by

$$G_j = \sum_{i=1}^{k} (n-n_i-1)$$

The overall error at the end of the conversion cycle becomes

$$\varepsilon_{\text{tot}} = \sum_{j=1}^{\ell} e_j G_j$$

However, one can observe that when the complete set of the DAC capacitors is used, the effect is a mismatch between input and integrating capacitors, giving a gain error. To distinguish the gain error from the non-linear term we measure mismatch with respect to the mean value of elements. Therefore

$$\sum_{i} e_i = 0$$

and the effective error caused by mismatch, referred to the input, becomes

$$\varepsilon_{\text{tot}} = \frac{2}{n(n-1)} \sum_{j=1}^{\ell} e_j (G_j - \max\{G\})$$

where the set of gains $G$ depends on input amplitude and element selection technique. The smart matching method aims at selecting unity elements so that

$$\max\{G\} = \min\{G\} + k$$

with $k$ minimum (possibly equal to 0).

Our selection algorithm obtains a minimum $k$ by balancing, along the conversion, the expected final weight of errors caused by each unity element. For that we use 8 indexes, $P_i(j)$ to denote the multiplying factor of each unity capacitance at the $j$-th conversion period. The values of $P_i(j+1)$ of the elements that are used at the clock time $j+1$ increases by $(n-j-2)$. Then, the set of elements is ordered with an increasing value of $P_i$. The set of $P_i$ is possibly diminished by the same amount to make its minimum equal to 0.

![Fig. 4 - Conceptual scheme of the 3-bit S-DEM.](image)

Fig. 4 shows the control logic’s flux with 8 register and $n=256$. The start of conversion sets the registers $P_i$ to zero. Suppose that the first input is 5. The elements used are the first 5 of the array and their index is set to 255. The sort moves them on the top so that the next input (4) selects 6-7-8-1. The fourth column shows the updated indexes. Since the minimum is 254, that value is subtracted to give the new-sorted indexes of the fifth column. An input equal to 5 produces new indexes that are scaled by 1, and so forth.

The control logic can be implemented with a limited number of gates and integrated on-chip to obtain the modulator shown in Fig. 5.

The S-DEM operates only on the first DAC because the gain of the first error from the second input to the output is much lower than the main DAC counterpart. If the input capacitance of the second stage is scaled, the mismatch can become important. In this case the designer can use a S-DEM control of the unity elements of the secondary DAC.

![Fig. 5 – Second order incremental with S-DEM.](image)
V. SIMULATION RESULTS

The S-DEM algorithm has been verified using the scheme of Fig. 5 and behavioral simulations. Since the DAC has 3-bit, the overall scheme obtains 18-bit and 20-bit with 256 and 512 clock periods respectively. The lower number of clock periods obtains a lower K(n) given by equation (1). This benefits a reduced value of the input capacitance bringing the unity element below 1 and 6pF for 1Vfs. Therefore, the design must use the most demanding request between matching accuracy and kT/C limit.

The key feature of this algorithm is the leveling along the conversion cycle of the error mismatch amplification resulting at the end of the conversion. The leveling depends on input amplitude. However, for better understanding the method, let us consider the input value that uses a single element every clock period. Without DEM the error of the first capacitor, $e_1$, is amplified by $n(n-1)/2$ as the input. Using the DWA-DEM and the S-DEM amplifies the gains of all the errors as shown in Fig. 6. The rotational sequence of the DWA-DEM gives rise to different amplifications of the various errors, as shown in Fig. 6 (n=256). At the end of the conversion the first gain is 224 more than the last, the second 192 and so forth. The quadratic superposition of those terms gives rise to an amplification by 378. The S-DEM performs better: for the selected input amplitude and n obtains a perfect balancing at the end of the conversion cycle.

For input values close to the reference limits the DWA-DEM becomes ineffective because the system takes a large number of cycles to complete a unity element rotation. The S-DEM preserves its effectiveness until the input amplitude enables a use of two times each element (or a two times use of all the elements minus one).

Running in parallel two incremental modulators one with matched elements and the other with a given random mismatch enables us to assess the S-DEM. Any difference between the digital results after the cascade of two integrators is considered an error. Actually that is not, strictly speaking, true because the output change can compensate for the quantization error and give rise to a more accurate result. However, since the compensation is not predictable we consider as error any difference.

Obviously, the digital difference is given by integer LSB and depends on the input amplitude and mismatches.

A run with an input staircase covering the full reference range gives rise to error histograms like the one of Fig. 6. Over a set of 800 samples we have a fractions of result with $\pm 1$ LSB difference. We assume that the method fully compensates the mismatch if the fraction of differences is less than 10%. The histogram of Fig. 6 is for 256 clock periods and random mismatch with $\sigma = 0.05\%$. The DWA-DEM method also grants a good improvement of the non-linearity but requires a higher matching to ensure the full compensation of mismatch. For the case of Fig. 7 it needs a $\sigma = 0.01\%$. Excellent performances are also obtained with n=512 (20-bit).

REFERENCES