Use of Time Variant Digital Sigma-Delta for Fractional Frequency Synthesizers

Victor R. Gonzalez-Diaz*, Aldo Pena Perez* and Franco Maloberti*
*Departament of Electronics
University of Pavia, Via Ferrata, 1 - 27100 Pavia - ITALY
Email: [victor.gonzalez, aldo.perez, franco.maloberti]@unipv.it

***Abstract*— This paper proposes a new low order time variant digital $\Sigma\Delta$ MASH modulator for fractional frequency synthesizers. The phase noise spectrum is improved as the spur tones from the fractional modulation are disabled. The usage of low order time variant MASH architectures reduces the number of levels that control the programable divider, reducing therefore the complexity and power requirements of the synthesizer.**

I. INTRODUCTION

PLL synthesizers generate fractional frequencies with very high resolution. A digital $\Delta\Sigma$ modulation converts the fractional part into a single or a multi-bit stream that pseudorandomly changes the division modulus [1] of the PLL loop, as shown in the block diagram of Fig. 1. The ratio between the $\Sigma\Delta$ input K and the full scale 2^m is the fractional value, that is $f_{out} = \left(N + \frac{K}{2^m}\right) f_{ref}$.

The goal of system designers is to use a low order $\Sigma\Delta$ architecture but to obtain smooth noise shaping so to reduce the phase noise [2]. Unfortunately, low order $\Sigma\Delta$ topologies give rise to signals with strong periodicity that, in turns, produce spur tones. This make it necessary to increase the $\Sigma\Delta$ order or to use stringent specifications in the loop filter. Moreover, the use of MASH schemes to obtain high order modulators increase the number of bits at output.

The necessity of long periods in the quantization error is attained with modifications of the digital accumulator so as to obtain a prime modulus quantization [3], [4], [5]. Unfortunately, for low order architectures the method is less effective. Other solutions foresee the addition of digital dither to input or to key points of the architecture [6]. However, dither is effective only for high order modulators [7]. In addition, generating long pseudorandom sequence requires cumbersome algorithms. Therefore, for obtaining low phase noise it is necessary to use high order $\Sigma\Delta$ and, consequently, many bits in the fractional divider.

This paper describes a method that ensures long bit stream periodicity with a low order digital MASH $\Sigma\Delta$. The solution is to change within time the modulator's coefficients. A multiplicative randomization of coefficients with dither significantly improves the pseudorandom characteristics. The programable divider uses less levels and thus the overall system requirements are relaxed. The remaining sections of the paper are organized as follows: Section II describes the method and some considerations to hardware implementation. In Section III and IV we present behavioral simulations in a fractional synthesizer to validate the method, finally we draw conclusions in Section V.

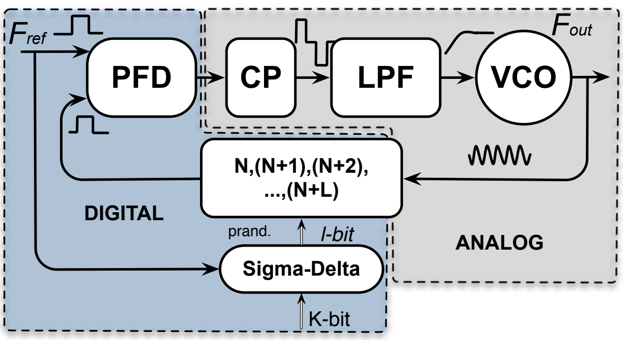


Fig. 1. A high resolution fractional synthesizer at block level.

II. METHOD TO INCREASE THE MASH PERIODICITY

The basic block of a digital MASH $\Sigma\Delta$ modulator is the accumulator. Critical input values cause repetitive patterns at the output. This method breaks the periodicity by changing in time the feedback coefficients in the accumulator as shown in Fig. 2. The delayed quantization error E_1, scaled by the factor $c_1 \ll 1$, is multiplied by a random sequence d_1 made by ± 1 and added to the quantization error. Possibly the result is truncated to m-bit to avoid increasing the accumulator length. The operation blurs the accumulation of the quantization error changing in time the Noise Transfer Function (NTF) from

$$NTF(z)_{zero} = (1 - z^{-1}) \tag{1}$$

to two extremes established by

$$NTF(z)_{shift} = \left[1 - (1 \pm c_1)z^{-1}\right]. \tag{2}$$

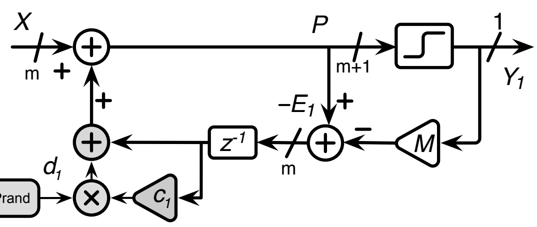


Fig. 2. Digital accumulator's model with time variant coefficient.

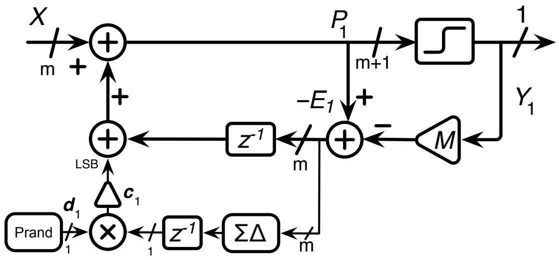


Fig. 3. Suggestion for the coefficient variation.

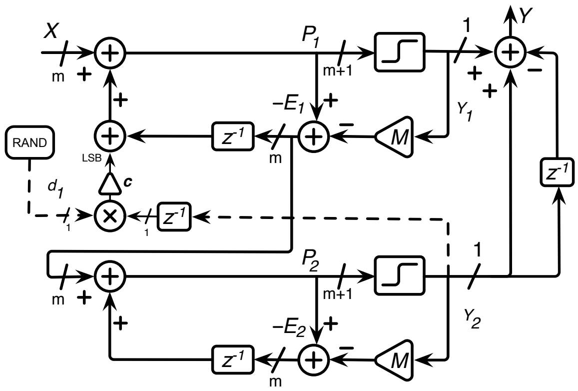


Fig. 4. The time variant MASH 1-1 ΣΔ implementation.

It is the mapping function of the digital accumulator that pseudorandomly changes and not the input that varies because of an additive term as it happens for the dithering.

The method is not very effective because requires using an expensive accumulator for the implementation. To obtain full benefits, the pseudo-random part operates the coefficient on the 1-bit transformation of the quantization error. A digital sigma-delta modulator, as shown in Fig. 3, performs the operation. Therefore, a simple AND gives rise to the 1-bit multiplication with the 1-bit PRNG.

The scheme requires an extra accumulator with the same number of bits of the quantization error. However, MASH architectures accumulate the quantization error of the previous stage for the quantization of that input, Therefore, the signal needed for the multiplication of the pseudo-random coefficient is available. Consider the Time Varian MASH 1-1 topology in Fig. 4. As the quantization error of the first accumulator is processed by the second one, the coefficient of the first accumulator is blurred just by feeding back the signal Y_2, and multiplying with the 1-bit pseudorandom signal d_1.

III. Computer Simulations

Behavioral computer simulations have verified the effectiveness of the time variant MASH. For performance comparisons simple and state-of-the-art solutions have been also considered. Fig. 5 shows the power spectral density of a traditional 8-bit MASH 1-1 ΣΔ modulator with input signal $X = 128$ made by only two tones. The same plot shows the result obtained with the addition of dither by an 8-bit LFSR [6], this

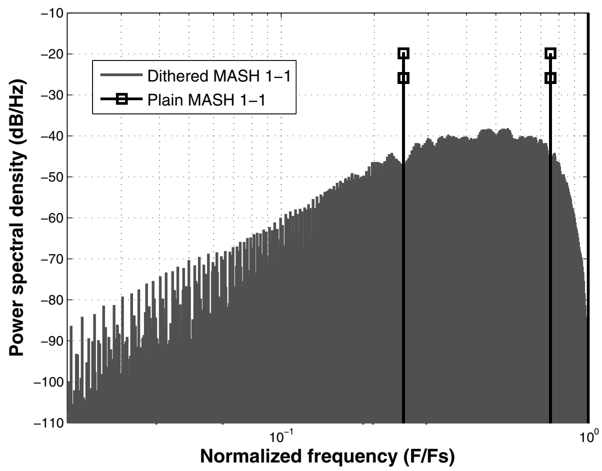


Fig. 5. Simulation results of traditional dithered MASH 1-1.

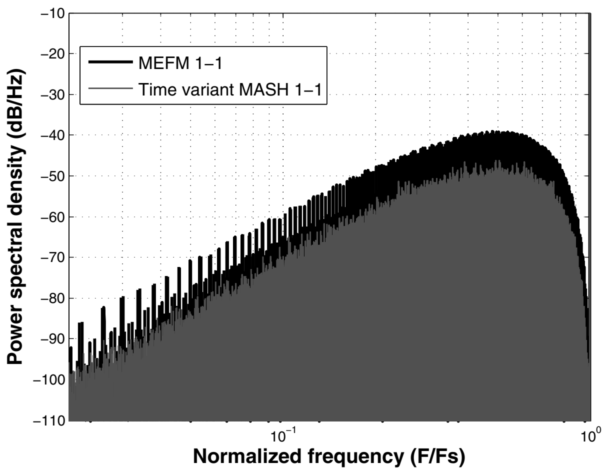


Fig. 6. Comparison between the MEFM and the proposed MASH 1-1.

significantly improves the result but still remains an envelope of tones which are related to the processing gain [8]. A recently proposed method called MEFM 1-1 [5] gives rise, in general, to better spectra with respect to the normal dither but for low order topologies still is not able to eliminate residual tones, as shown in Fig. 6. The same figure reports the spectrum of the proposed time variant MASH 1-1 of Fig. 4. Both of them use 8-bit accumulators but the MEFM needs additional processing and the proposed MASH 1-1 uses only the extra 8-bit LFSR. It is evident that the time variant spectrum is much more noise-shaped like with spur tones reduced by about 10 dB.

The quality of the spectrum obtained by the time variant MASH 1-1 is comparable with a dithered MASH 1-1-1. This is significant because the use of a lower order modulator gives rise to less bits the programable divider's input used in a fractional synthesizer; namely, 4 levels for a MASH 1-1 instead then the 8-level MASH 1-1-1.

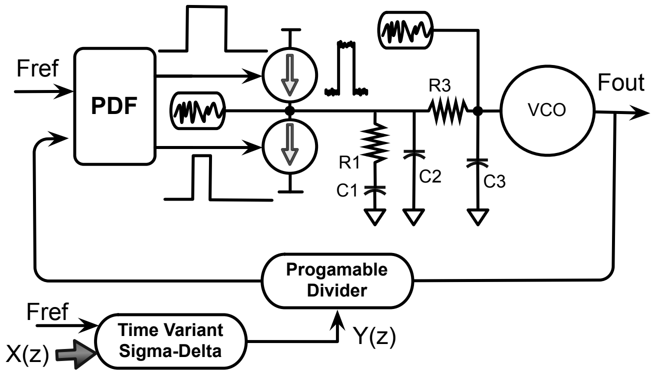


Fig. 7. Conception of the behavioral model in VerilogA.

TABLE I
SIMULATED FRACTIONAL SYNTHESIZER PARAMETERS.

Parameter	Value	Parameter	Value
K_{VCO}	$666\ \frac{MHz}{V}$	I_{CP}	$10\ \frac{\mu A}{V}$
$S_{pfdcp}(f)$	$1.6x10^{-24}\ \frac{A^2}{Hz}$	$S_{lfvco}(f)$	$2x10^{-22}\ \frac{V^2}{HZ}$
f_{ref}	$25\ MHz$	f_c	$270\ KHz$
LPF	3rd order	Division	$N = (64..79)$

IV. Fractional Synthesizer with Time-variant ΣΔ

The superior output spectra obtained by time variant MASH 1-1 indicate a possible benefit for its use in fractional synthesizers. This has been verified at the behavioral level with a compete model written in VerilogA. The model, whose block diagram is shown in Fig. 7, also accounts for noise in the charge-pump and in Voltage Controlled Oscillator (VCO). The model parameters are VCO gain K_{VCO}, charge pump current I_{CP}, charge pump input refereed noise S_{pfdcp}, VCO input refereed noise S_{lfVCO}, reference frequency f_{ref} and loop filter's cut off frequency f_c. The model also describes the Phase to Frequency Detector (PFD) with a zero dead zone to highlight the $\Sigma\Delta$ periodicity's impact on the response. A p-welch algorithm calculates the PSD. The simulator uses 2^{22} sample points to obtain the necessary resolution to detect hidden tones. Table I gives the numerical values used in the performed simulations.

The use of a programmed frequency equal to $f_{out} = \left(67 + \frac{77}{256}\right)$ shows that the time variant method improves the performance even for non prime constant inputs. Fig. 8 compares the PSD with a third order MASH 1-1-1 and a second order time variant MASH 1-1. The plot highlights the spectrum improvement in terms of reduction of tones. Similar benefits result in the phase noise as shown in Fig. 9. The time variant MASH 1-1 with the same loop filter improves the performance by 20dB at intermediate frequencies.

A more stringent simulation with a MASH 1-1-1, dithered with a 16-bit LFSR on the second stage, is compared to obtained results. Fig. 10(a) shows that the time variant MASH 1-1 gives rise to an improved spectrum (this is due to the smoother noise shaping). When obtaining the phase noise figure in Fig. 10(b), the dithered MASH 1-1-1 presents tones at low frequencies offset from the carrier. The tones for the dithered solution appear at low frequencies where the charge pump noise is dominant.

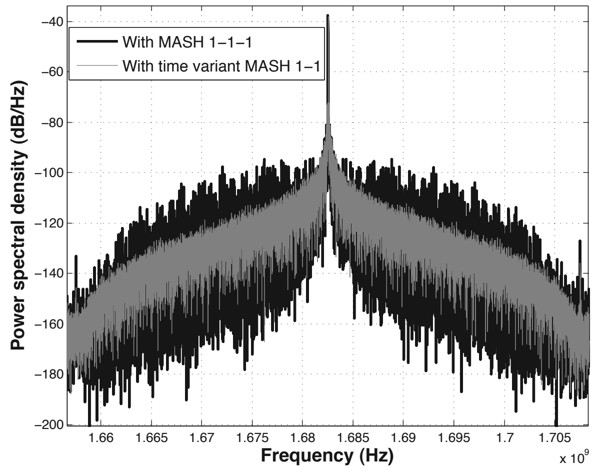


Fig. 8. PSD results from the verilogA model comparing a plain MASH 1-1-1 and proposed Time Variant MASH 1-1.

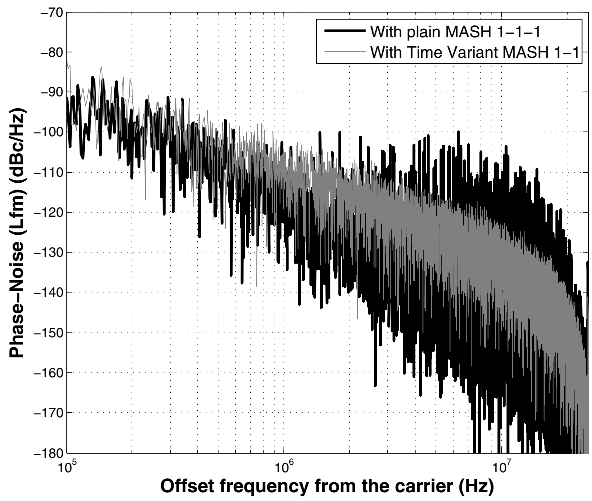
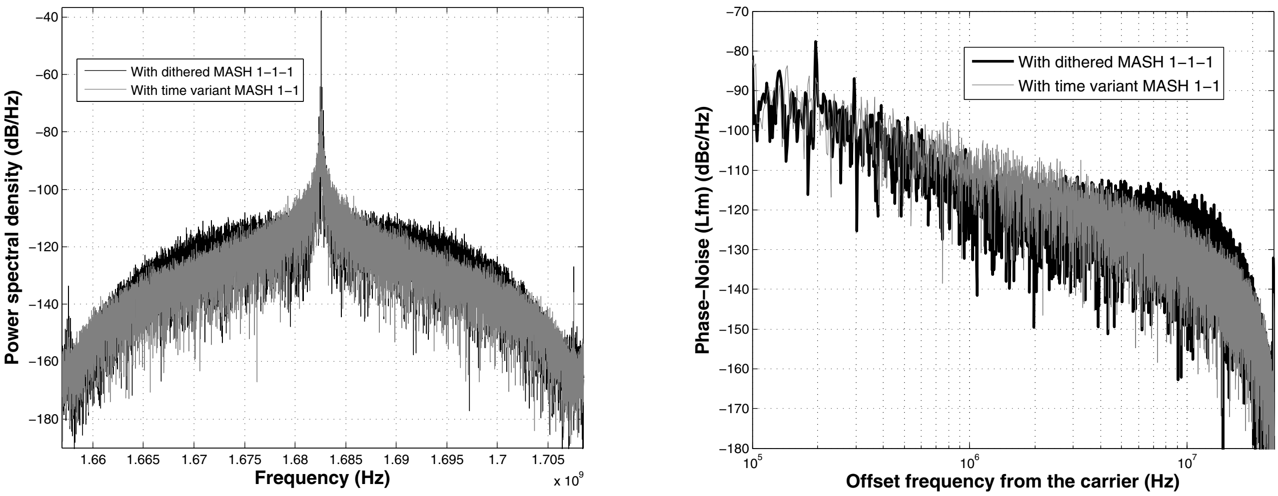


Fig. 9. Phase noise figured obtained from the plain MASH 1-1-1 and proposed Time Variant MASH 1-1.

The origin of spur tones are due to the hidden dithered MASH 1-1-1 periodicity not visible in the spectrum of the sigma-delta output because they occur where the noise is large. These tones get mixed and produce products at lower frequencies. This is the supposed possible origin as, for this model, the PFD causes non-linearity being described with a zero dead zone. The result confirms a previous publication on the method stating that the time variant $\Sigma\Delta$ approach is beneficial when applied to non linear systems [8], as the output periodic behavior is reduced.

In addition to tones reduction the time variant $\Sigma\Delta$ mod-



(a) Power spectrum.

(b) Phase noise figure.

Fig. 10. Fractional synthesizer verilogA simulation results to compare the proposed method with a third order dithered MASH.

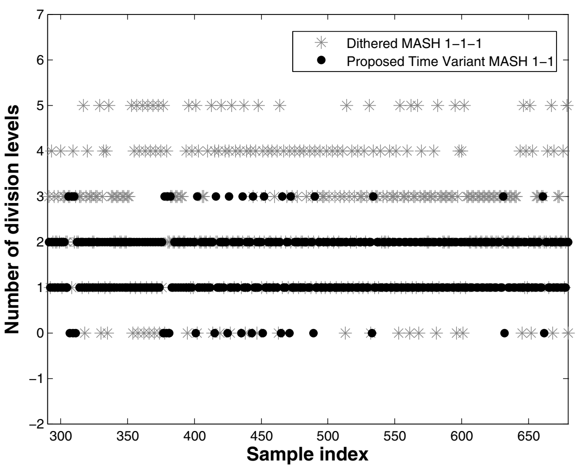


Fig. 11. Number of divider's levels in the fractional synthesizer for a traditional dithered MASH 1-1-1 and the proposed TV MASH 1-1.

ulation allows a reduction of the number of levels in the programable divider. Fig. 11 shows the number of levels used for a traditional MASH 1-1-1 and for the TV-MASH 1-1. With a reduction of levels from 6 to 4, programable divider's complexity is reduced and therefore the design complexity and power requirements.

V. Conclusion

A new solution that reduces spur tones of a digital $\Sigma\Delta$ modulator is proposed. The method consists on varying along time the coefficients of MASH $\Sigma\Delta$ modulator to disable the quantization noise periodicity. The proposed solution has been explored at behavioral level to demonstrate that second order time variant MASH has better performance than previous techniques that use third order modulators with constant input, even at critical inputs. A significant benefit with a second order with better performance is that it reduces the programable divider complexity which is one of the most power consuming blocks of a fractional frequency synthesizer.

References

[1] T. A. D. Riley, M. A. Copeland, and T. A. Kwasniewski, "Delta-Sigma Modulation in Fractional-N Frequency Synthesis," *IEEE J. Solid-State Circuits*, vol. 28, no. 5, pp. 553–559, may 1993.

[2] M. H. Perrot, M. D. Trott, and C. G. Sodini, "A Modeling Approach for $\Sigma\Delta$ Fractional-N Frequency Synthesizer Allowing Strightforward Noise Analysis," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp. 1028–1038, aug 2002.

[3] M. J. Borkowski and J. Kostamovaara, "Spurious Tone Free Digital Delta-Sigma Modulator Design for DC Input," in *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS'05)*, May 2005, pp. 5601–5604.

[4] J. Liu, H. Liao, R. Huang, and X. Zhang, "Sigma-Delta Modulator with Feedback Dithering for RF Fractional-N Frequency Synthesizer," in *Proceedings of the 2005 IEEE Conference on Electron Devices and Solid-State Circuits*, Dec. 2005, pp. 137–139.

[5] K. Hosseini and M. P. Kennedy, "Architectures for Maximum Sequence Lenght Digital Delta-Sigma Modulators," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 12, pp. 1104–1108, nov 2008.

[6] S. Parmati, J. Welz, and I. Galton, "Statistics of the Quantization Noise in 1-Bit Dithered Single-Quantizer Digital Sigma-Delta Modulators," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 3, pp. 492–503, mar 2007.

[7] V. R. Gonzalez-Diaz, M. Garcia-Andrade, G. Espinosa, and F. Maloberti, "Efficient Dithering in MASH Sigma-Delta Modulators for Fractional Frequency Synthesizers," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 9, pp. 2394–2403, sep 210.

[8] F. Maloberti, E. Bonizzoni, and A. Surano, "Time Variant digital Sigma-Delta Modulator for Fractional-N Frequency Synthesizers," in *Proceedings of the IEEE International Symposium on Radio-Frequency Integration Technology, RFIT 2009*, Dec. 2009, pp. 111–114.