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A Novel Implementation of Dithered Digital Delta-Sigma Modulators via Bus-Splitting

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***Abstract*—This paper presents a design methodology for dithered bus-splitting Multi stAge noise SHaping (MASH) digital delta-sigma modulators (DDSMs). Rules for selecting the appropriate wordlengths of the constituent DDSMs are derived which ensure that the spectral performance of the bus-splitting architecture is comparable to that of the conventional design but with less hardware. Behavioral simulations are presented which confirm the theoretical predictions.**

I. Introduction

Quantization noise shaping via digital delta-sigma modulation is a widely used technique in the fields of data converter, fractional-N frequency synthesizer, and all-digital phase-locked loop (ADPLL) design. In a DDSM, a high resolution discrete-time input is oversampled and requantized to produce a lower resolution output while the power of resulting quantization noise is suppressed within some frequency band of interest.

The focus of recent research has been on developing techniques to ensure that the DDSM output spectrum is free of spurious tones. Cycle length extension approaches minimize the quantization noise power per tone when the input is constant [1], [2]. On the other hand, the stochastic LSB dithering technique has been shown to eliminate spurious tones in the DDSM's output spectrum provided that the dither undergoes two or more integrations on the way to the quantizer [3], [4]. In this paper, we focus on the stochastic technique.

A design methodology based on error masking has been developed and applied to MASH DDSMs, reducing the hardware requirement by up to 20% without sacrificing performance [5]. In this work, we investigate a bus-splitting idea for implementing dithered DDSMs, in which the digital input word to a high order DDSM is partitioned into a number of parts and the LSBs are processed by one or more low order DDSMs before being recombined with the MSBs. Our work is inspired by the ideas of Norsworthy *et al.* [6] and uses the error masking technique developed in [5].

II. MASH DDSM Architecture

The basic building block of the MASH DDSM we consider in this work is the first-order error feedback modulator (EFM1) shown in Fig. 1. The input to the modulator is a digital word

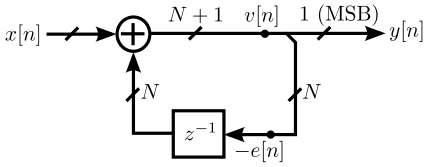


Fig. 1. Block diagram of a first-order error feedback modulator (EFM1).

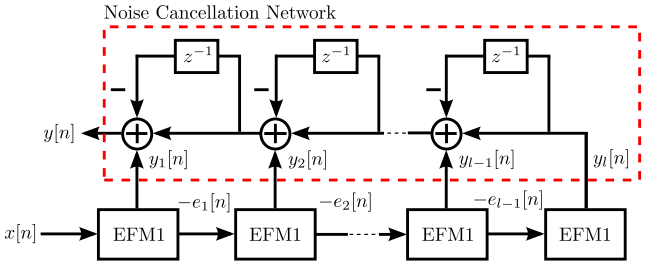
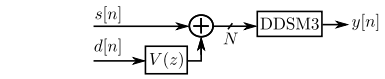


Fig. 2. Block diagram of an l^{th} order MASH DDSM incorporating a cascade of EFM1s

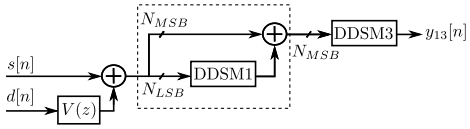
with N bits. The 1-bit quantization is achieved by taking the MSB of $v[n]$. The discarded LSBs, representing the negative of the quantization error ($-e[n]$), are then fed back and summed with the input.

Figure 2 shows a block diagram of a conventional l^{th} order MASH DDSM comprising a cascade of l N-bit EFM1 blocks and a noise cancellation network. In this structure, the negative of the quantization error from each stage ($-e_i[n]$) is fed to the next stage and the output of each stage ($y_i[n]$) is fed to the noise cancellation network, which eliminates the intermediate quantization noise terms. We will denote an l^{th} order MASH DDSM by DDSMl.

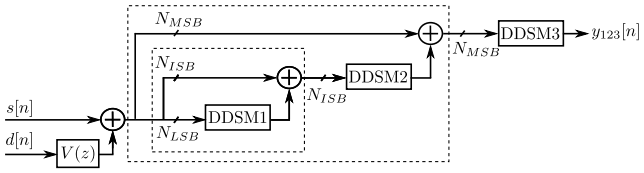
Figure 3(a) shows a simplified block diagram of the dithered DDSM3 that we consider in this work. In this scheme, a 1-bit dither sequence, d, high-pass filtered by a shaping filter $V(z) = (1 - z^{-1})^R$, is added to the desired signal, s. It has been proven that the quantization noise is white, uniformly distributed and independent of the DDSM input if $R \leq l - 2$, where l is the order of the MASH DDSM [4]; this ensures a spur-free output spectrum. Consequently, in the case of third-



(a) Dithered DDSM3



(b) Dithered bus-splitting 1-3 DDSM3



(c) Dithered nested bus-splitting 1-2-3 DDSM3

Fig. 3. The dithered DDSM3 (a), the dithered bus-splitting 1-3 DDSM3 (b), and the dithered nested bus-splitting 1-2-3 DDSM3 (c).

order MASH DDSMs, both non-shaped ($R = 0$) and first-order shaped ($R = 1$) dither can be used to suppress spurs.

Assuming white quantization noise, the noise at the output can be estimated using the traditional linear model [5]

$$\mathcal{L}(f) = \frac{\Delta^2}{12} \left| NTF(z) \right|^2_{z=e^{j2\pi f/f_s}}, \tag{1}$$

where Δ is the quantization interval, $NTF(z)$ is the noise transfer function which shapes the quantization noise, and f_s is the (uniform) sampling frequency.

III. Design Methodology

Consider the dithered bus-splitting architectures shown in Figs. 3(b) and 3(c) where the digital input word is split into different parts. We present the design methodology of the dithered nested bus-splitting 1-2-3 DDSM3 in detail and provide a design equation for the bus-splitting 1-3 DDSM3. The PSDs of the filtered error signals N_1, N_2, and N_3 from DDSM1, DDSM2, and DDSM3, respectively, can be approximated by

$$\mathcal{L}_1(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{MSB}+N_{ISB}}} \right)^2 \left| (1 - z^{-1}) \right|^2_{z=e^{j2\pi f/f_s}}, \tag{2}$$

$$\mathcal{L}_2(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{MSB}}} \right)^2 \left| (1 - z^{-1})^2 \right|^2_{z=e^{j2\pi f/f_s}}, \tag{3}$$

$$\mathcal{L}_3(f) = \frac{1}{12} \left| (1 - z^{-1})^3 \right|^2_{z=e^{j2\pi f/f_s}}. \tag{4}$$

A. Zeroth-Order Dither

In the case of a DDSM with zeroth-order LSB dithering and a constant input, the low frequency noise floor is determined by the dither signal. In the case of zeroth-order dither, the level of the noise floor is [5]

$$\mathcal{L}_{nf0}(f) = \frac{1}{12} \left(\frac{1}{2^N} \right)^2, \tag{5}$$

and the largest frequency at which the PSD of the dithering is larger than the contribution from the shaped quantization error of DDSM3 is given by

$$f_0 = \frac{1}{\pi \cdot 2^{N/3}} \cdot \frac{f_s}{2}. \tag{6}$$

Figure 4 shows typical contributions $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$, and $\mathcal{L}_{nf0}$ for a zeroth-order dithered nested bus-splitting 1-2-3 DDSM3. The corner frequency f_0 is defined by the intersection of $\mathcal{L}_3$, and $\mathcal{L}_{nf0}$. As $\mathcal{L}_1$ and $\mathcal{L}_2$ are first- and second-order shaped, respectively, we require that

$$\mathcal{L}_1 < \mathcal{L}_3 @ f_0 \quad \text{and} \quad \mathcal{L}_2 < \mathcal{L}_3 @ f_0 \tag{7}$$

to mask the quantization error of the intermediate DDSMs below that of the dithering and the error from DDSM3.

We can approximate $\mathcal{L}_1$, $\mathcal{L}_2$, and $\mathcal{L}_3$ at low frequencies by

$$\mathcal{L}_1(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{MSB}+N_{ISB}}} \right)^2 \cdot 2^2 \left(\frac{\pi f}{f_s} \right)^2, \tag{8}$$

$$\mathcal{L}_2(f) = \frac{1}{12} \cdot \left(\frac{1}{2^{N_{MSB}}} \right)^2 \cdot 2^4 \left(\frac{\pi f}{f_s} \right)^4, \tag{9}$$

$$\mathcal{L}_3(f) = \frac{1}{12} \cdot 2^6 \left(\frac{\pi f}{f_s} \right)^6. \tag{10}$$

Substituting (8), (9), and (10) into the constraints (7) and solving yields

$$N_{MSB} + N_{ISB} > \frac{2N}{3} \tag{11}$$

$$N_{MSB} > \frac{N}{3}. \tag{12}$$

A similar analysis can be performed to determine the optimum wordlengths for the bus-splitting 1-3 DDSM3 with zeroth-order dither. In order to design a bus-splitting MASH DDSM

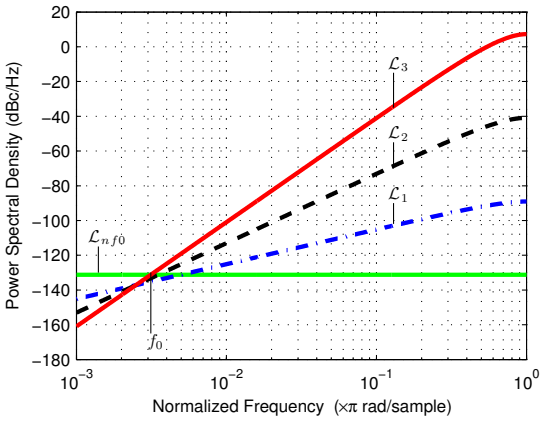


Fig. 4. Masking (dashed-dotted) $\mathcal{L}_1$ and (dashed) $\mathcal{L}_2$ below (solid) $\mathcal{L}_3$ at f_0. $\mathcal{L}_1$, $\mathcal{L}_2$, $\mathcal{L}_3$ and $\mathcal{L}_{nf0}$ are defined by (2)–(4) and (5). In this example, $N_{LSB} = 6$, $N_{ISB} = 7$, and $N_{MSB} = 7$.

TABLE I
OPTIMIZED WORDLENGTHS FOR BUS-SPLITTING DDSM3 ARCHITECTURES

Nested DDSM	Wordlengths		
	N_{LSB}	N_{ISB}	N_{MSB}
(a) 1-3	N-M	-	M
(b)1-2-3	N-M	M-L	L

with a PSD similar to that of a conventional N-bit MASH DDSM3 with zeroth-order dither, the design procedure is as follows:

- Choose the desired bus-splitting architecture and determine the optimized wordlengths from Table I using $M = \lceil \frac{2N}{3} \rceil$ and $L = \lceil \frac{N}{3} \rceil$ where appropriate.

B. First-Order Dither

If first-order shaped dither is applied to the input of the DDSM, its noise floor is defined by

$$\mathcal{L}_{nf1}(f) = \frac{1}{12}\left(\frac{1}{2^N}\right)^2 |2\sin(\pi f/f_s)|^2 \qquad (13)$$

and the largest frequency at which the PSD of the dithering is larger than the contribution from e_3 is given by

$$f_1 = \frac{1}{\pi \cdot 2^{N/2}} \cdot \frac{f_s}{2}. \qquad (14)$$

Figure 5 shows typical contributions $\mathcal{L}_2$, $\mathcal{L}_3$, and $\mathcal{L}_{nf1}$ for a first-order dithered nested bus-splitting 1-2-3 DDSM3. The key frequency in this case, f_1, is defined by the intersection of $\mathcal{L}_3$, and $\mathcal{L}_{nf1}$. Note that we have not shown $\mathcal{L}_1$ in Fig. 5. Since $\mathcal{L}_1$ is first-order shaped, we require that $\mathcal{L}_1 < \mathcal{L}_{nf1}$, which reduces to

$$N_{MSB} + N_{ISB} \geq N. \qquad (15)$$

Since our objective is to *minimize* the overall hardware requirement, we choose $N_{MSB} + N_{ISB} = N$.

Recall that $N_{MSB} + N_{ISB} + N_{LSB} = N$ by definition; hence $N_{LSB} = 0$. Thus, (15) implies that it is not necessary to use a first-order DDSM to shape the N_{LSB} bits of the input word. In this case, a nested bus-splitting 1-2-3 DDSM3 reduces to a bus-splitting 2-3 DDSM3.

Next, $\mathcal{L}_2$ needs to be masked by $\mathcal{L}_3$, as shown schematically in Fig. 5. Thus, the word-length strategy for the DDSM2 requires that

$$\mathcal{L}_2 < \mathcal{L}_3 @ f_1 \qquad (16)$$

Substituting (9), (10), and (14) into (16) and solving yields

$$N_{MSB} > \frac{N}{2}. \qquad (17)$$

In order to design a bus-splitting 2-3 DDSM3 with a PSD similar to that of a conventional N-bit MASH DDSM3 with first-order dither, the design procedure is as follows:

- Choose $N_{MSB} = \lceil \frac{N}{2} \rceil$.
- Choose $N_{ISB} = N - N_{MSB}$.

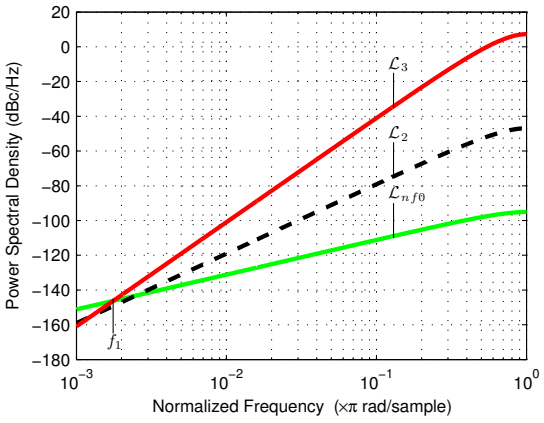


Fig. 5. Masking (dashed) $\mathcal{L}_2$ below (solid) $\mathcal{L}_3$ at f_1. $\mathcal{L}_2$, $\mathcal{L}_3$ and $\mathcal{L}_{nf1}$ are defined by (3), (4) and (13). In this example, $N_{LSB} = 0$, $N_{ISB} = 9$, and $N_{MSB} = 11$.

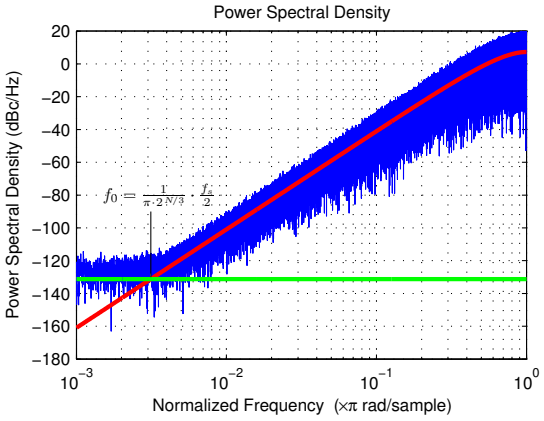


Fig. 6. Simulated PSD at the output of a zeroth-order dithered 20-bit MASH DDSM3; the input is 104857. The smooth curves are $\mathcal{L}_3$ (2) and $\mathcal{L}_{nf0}$ (5).

IV. DESIGN EXAMPLES

Next we present a design example for a zeroth-order dithered 20-bit MASH DDSM3. The appropriate wordlengths for the nested bus-splitting 1-2-3 DDSM3 are $N_{MSB} = 7$, $N_{ISB} = 7$, and $N_{LSB} = 6$. The spectral performance of the architectures are evaluated using MATLAB behavioral simulations of the modulators with 2^{20} output samples.

The simulated PSD for a conventional zeroth-order dithered 20-bit MASH DDSM3 is shown in Fig. 6. The PSD of the 7-7-6-bit nested bus-splitting 1-2-3 DDSM3 is shown in Fig. 7. Note that the N_1 and N_2 components lie below the spectral envelope of N_3 above f_0 and are therefore masked by it, as expected. Consequently, N_1 and N_2 do not affect the overall performance of the nested bus-splitting 1-2-3 DDSM3.

The hardware requirements for (i) a conventional 20-bit MASH DDSM3 and (ii) the bus-splitting DDSM architectures with zeroth-order dither are summarized in Table II. The hardware consumption is reported as the number of flip-flops (FFs), the number of four-input lookup tables (LUTs), and the total-equivalent-gate (TEG) count. Note that the hardware

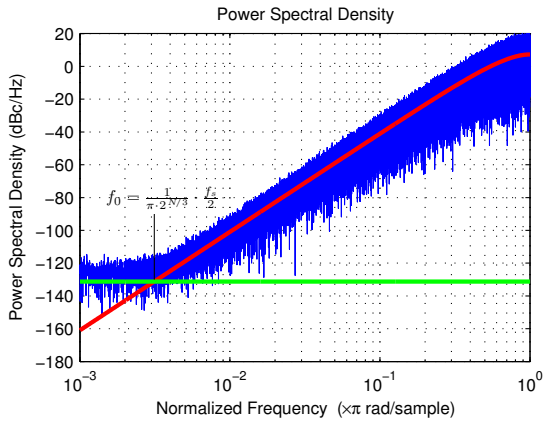


Fig. 7. Simulated PSD at the output of a zeroth-order dithered 7-7-6-bit nested bus-splitting 1-2-3 DDSM3; the input is 104857. The smooth curves are $\mathcal{L}_3$ (2) and $\mathcal{L}_{nf0}$ (5).

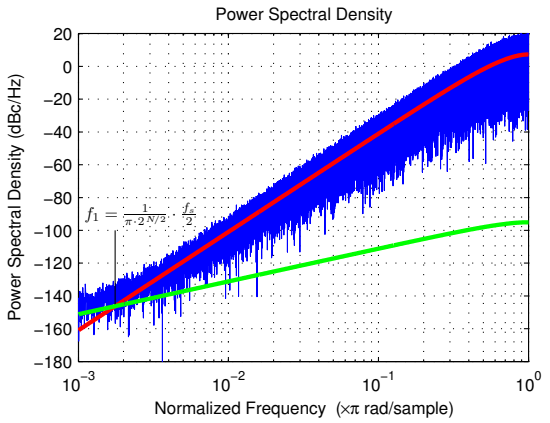


Fig. 8. Simulated PSD at the output of a first-order dithered 20-bit MASH DDSM3; the input is 3277. The smooth curves are $\mathcal{L}_3$ (2) and $\mathcal{L}_{nf1}$ (13).

TABLE II
HARDWARE CONSUMPTION OF A CONVENTIONAL 20-BIT MASH DDSM3 AND THE NESTED BUS-SPLITTING DDSM WITH ZEROTH-ORDER AND FIRST-ORDER DITHER

MASH DDSM with dither	Hardware Consumption		
	FFs	LUTs	TEG
(a) Conventional 20-bit	63	66	1251
(b) 14-6-bit 1-3 bus-splitting	51	54	1011
((b)/(a))%	81%	82%	81%
(c) 7-7-6-bit 1-2-3 nested bus-splitting	45	55	963
((c)/(a))%	71%	87%	77%
(d) 11-9-bit 2-3 bus-splitting	55	69	1193
((d)/(a))%	87%	105%	95%

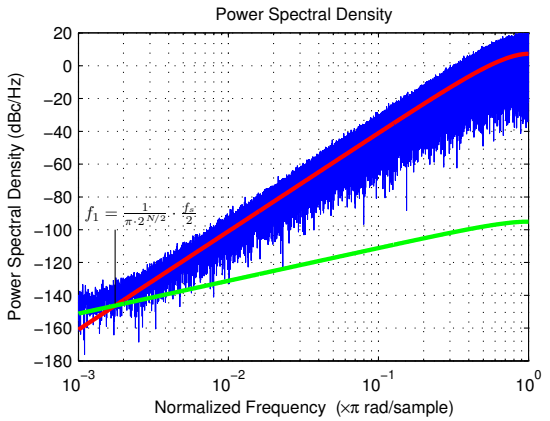


Fig. 9. Simulated PSD at the output of a first-order dithered 11-9-bit bus-splitting 2-3 DDSM3; the input is 3277. The smooth curves are $\mathcal{L}_3$ (2) and $\mathcal{L}_{nf1}$ (5).

requirement of the dither block has been excluded in order to allow a direct comparison of the relative hardware consumption of the bus-splitting architectures. Hardware savings of 19% and 23% are achieved in the case of the bus-splitting 1-3 DDSM3 and nested bus-splitting 1-2-3 DDSM3, respectively.

The simulated PSD for a conventional 20-bit MASH DDSM3 with first-order additive input dither is shown in Fig. 8. Applying the design equation (17), the wordlengths of the bus-splitting 2-3 DDSM3 are $N_{MSB} = 11$ and $N_{ISB} = 9$. The simulated PSD for the 11-9-bit bus-splitting 2-3 DDSM3 is shown in Fig. 9. As expected, the bus-splitting DDSM3 achieves an almost identical PSD compared to the conventional 20-bit MASH DDSM3. The hardware requirements for the bus-splitting 2-3 DDSM3 architecture with first-order dither are also summarized in Table II and show a saving of 5%.

V. CONCLUSION

In this paper, we have presented a design methodology for dithered bus-splitting MASH DDSMs based on error masking which exploits the shape of the noise floor when dither is applied to the input to reduce the hardware requirement *without* sacrificing performance. Using this technique, hardware savings of 23% and 5% can be achieved in the cases of zeroth-order and first-order shaped dither, respectively.

ACKNOWLEDGMENT

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