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Mono-Rate and Multi-Rate Hybrid Continuous-Time $\Sigma\Delta$ Modulators with SC Feedback DAC

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***Abstract*—Methods for avoiding the slew-rate limit and the optimal design of hybrid Continuous-Time (CT) $\Sigma\Delta$ modulators with switched-capacitor (SC) DAC are discussed. Limitations on performance due to finite bandwidth and slew-rate of the operational amplifier are analyzed. The use of multi-rate scheme made by a set of time-interleaved SC-DAC moderates the non-linear error caused by the limited slew-rate in mono-rate converter at equal slew-rate. Behavioral level simulations confirm the validity of proposed technique.**

I. Introduction

A continuous time (CT) $\Sigma\Delta$ modulator operates better than its discrete time (DT) counterpart in terms of speed, implicit anti-aliasing, and power consumption. By contrast, CT modulators are difficult to design, are sensitive to the clock jitter, [1], and are limited by the non-linear response of the used elements. The non-linear limit, dominated by the first integrator, is normally solved by using an RC integrator as first stage, possibly followed by g_mC stages. The clock jitter sensitivity is resolved by the use of DACs with decaying pulses, like the exponentially shaped waveform generated by a modified switched capacitor circuit (SC-DAC), [2], [3]. If the exponential goes to zero the charge injected by the DAC is jitter independent. If there is a small fraction of charge that remains on the capacitor the jitter error diminishes as the ratio between the initial and the final charge on the injecting capacitor.

The use of an hybrid integrator with a resistance on the signal path and a SC scheme for realizing the DAC avoids jitter dependency but causes errors if the op-amp bandwidth is finite and the slew-rate limited. The two real dependencies give rise to a linear and a non-linear error. Since a linear error is equivalent to integrator gain error, the main concern is for the non-linear term. This paper analyzes the limit that causes non-linearity and proposes method for its reduction or cancellation. The most effective solution is the use of a multi-rate hybrid scheme. Performances are studied with analytical considerations and verified by behavioral simulations.

This paper is organized as follows. Section II describes and discusses hybrid continuous time $\Sigma\Delta$ modulators. Section III presents three possible techniques to avoid non-linear responses. Simulation results given in Section IV demonstrate that the multi-rate approach ensures superior performances.

II. Hybrid Continuous-Time $\Sigma\Delta$ Modulator

Fig. 1 shows a hybrid continuous-time $\Sigma\Delta$ modulator. The continuous-time path made by the resistance R_1 gives rise to the integration of the input signal, V_{in}. The feedback path is a switched-capacitor (SC) network made by switches with on-resistance R_{on}. Let us suppose $C_1 = C_2$ and gain of the integrator equal to 1. It results $R_1C_1 = T_S$. The capacitance C_L accounts for the capacitive load of the next stage and the compensation capacitance of the op-amp. Immediately after phase Φ_2 rises, the op-amp does not react and the virtual ground and output voltages change just because of the capacitive coupling established by C_2, C_1 and C_L. The virtual ground and output voltage become

$$V_{vg} = V_{DAC}\frac{C_2}{C_2 + C_1C_L/(C_1 + C_L)} = \alpha V_{DAC}; \quad (1)$$

$$V_{out} = V_{DAC}\frac{C_1C_2/(C_1 + C_2)}{C_L + C_1C_2/(C_1 + C_2)} = \beta V_{DAC}; \quad (2)$$

where V_{DAC} is the voltage of the DAC.

After there is a transient of output and virtual ground voltages associated to the integration of the charge of C_2 into C_1. If the input voltage is zero, the virtual ground goes to zero, otherwise it settle to about $V_{vg}(\infty) \approx V_{in}/(g_mR_1)$ (g_m is the transconductance gain of the op-amp).

The transients depend whether the operational amplifier is in slew-rate or not. When the input differential voltage is

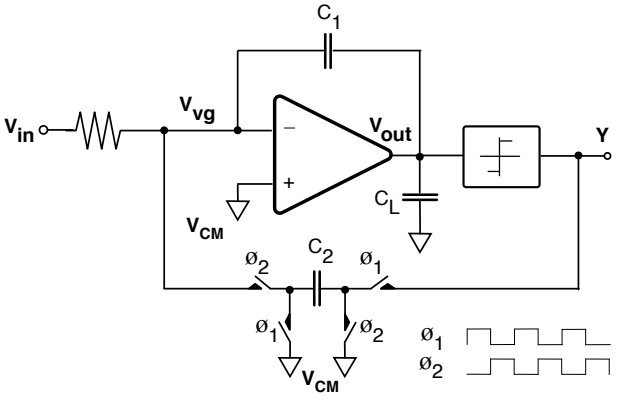

Fig. 1. Block diagram of a hybrid CT modulator.

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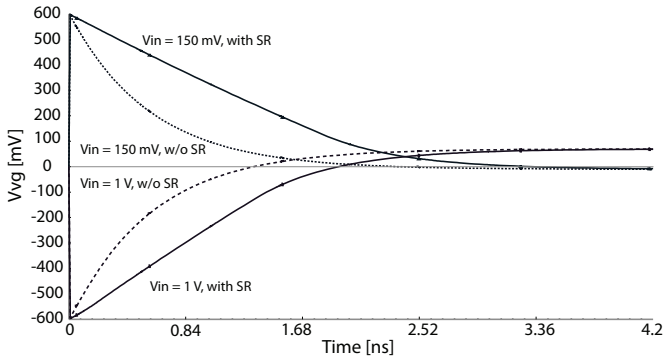

Fig. 2. Simulated virtual ground waveforms with and without slew-rate limitation for two input voltage values.

higher than $\sqrt{2}V_{ov}$ (V_{ov} is the overdrive voltage of the input differential pair), the input stage is completely unbalanced and the output current and the bias conditions and the used scheme determine the current at output of the op-amp. Typically the current is less than a given value, I_{SR}. If V_{vg} is lower than $\sqrt{2}V_{ov}$, the waveforms change exponentially (supposing to model the op-amp with a single pole model). If V_{vg} exceeds $\sqrt{2}V_{ov}$, the op-amp goes in slewing until the input difference becomes lower than $\sqrt{2}V_{ov}$. Until then, the waveforms change almost linearly, then they decrease exponentially.

In the slew-rate condition $|I_{out}| > I_{SR}$. Accounting for the current from resistance R_1, the discharge current of the SC capacitor C_2 is approximated by

$$I_{C_2} = \frac{V_{in} - V_{vg}}{R_1} - C_L \frac{dV_{out}}{dt} - I_{SR}; \tag{3}$$

that, together with other equations, describes the transient during slewing. Fig. 2 shows the virtual ground waveform for two values of input voltage (V_{in} = 1 V and V_{in} = 150 mV), supposed constant, and a positive or negative DAC output ($|V_{DAC}|$ = 1 V). The figure also shows waveforms for the case of infinite slewing. They are exponentials that approximately settle to $V_{vg}(\infty)$. For finite slew-rate, the linear part ends at a time that depends on the value of the input voltage.

What is relevant for our study is that the virtual ground does not remain at a constant level, [4], and this changes the current of the input resistance by $(V_{in} - V_{vg})/R_1$. The consequence is an extra fraction of injected charge, ΔQ, inversely proportional to the the input resistance, R_1.

Supposing $t = 0$ the beginning Φ_2 and $\bar{t}$ the time at which the op-amp exits from the slewing condition, the lost charge is

$$\Delta Q_{SR} = \int_0^{\bar{t}} \frac{V_{vg}(t)}{R_1} dt. \tag{4}$$

When the op-amp is in the linear region the virtual ground settles to $V_{vg}(\infty)$ exponentially with a time constant, τ_1, that depends on capacitances and transconductance gain of the op-amp. To be precise, we should also account for the on resistance of the switches. If the period of phase 2 is long enough, the virtual ground voltage reaches its asymptotical value. ΔQ in the interval $(\bar{t} \cdots T_S/2)$ can be calculated as

$$\Delta Q_{exp} = \int_{\bar{t}}^{\infty} \frac{V_{vg}(t) e^{-(t-\bar{t})/\tau_1}}{R_1} dt = \frac{\sqrt{2}V_{ov} \cdot \tau_1}{R_1} \tag{5}$$

being $V_{vg}(\bar{t}) = \sqrt{2}V_{ov}$. If the virtual ground voltage does not settle to zero, the integral of equation (5) further depends on V_{in} because $\bar{t}$ affects the integral (5).

The total extra charge injected into the virtual ground becomes

$$\Delta Q_{slew}(V_{in}) = \Delta Q_{SR}(V_{in}) + \Delta Q_{exp}(V_{in}) \tag{6}$$

If the value of $V_{vg}(0)$ established by equation (1) is lower than the slew-rate limit, the virtual ground voltage starts immediately an exponential decrease, giving rise to a lost charge equal to

$$\Delta Q_{no\text{–}slew} = \int_0^{\infty} \frac{V_{vg}(0) e^{-t/\tau_1}}{R_1} dt = \frac{\alpha V_{DAC} \tau_1}{R_1}. \tag{7}$$

Since $\Delta Q_{no\text{–}slew}$ does not depend on the input voltage, the error corresponds to a DAC gain error. Even if the virtual ground does not settle to zero $\Delta Q_{no\text{–}slew}$ is constant. Moreover, the SC capacitor C_2 is not completely discharged. The error is constant and can be incorporated in a DAC gain error and it can be easily compensated for by tuning the injection coefficient.

From the above, we notice that what is relevant is the non-linear part caused by slewing and input voltage. It is zero if the op-amp does not slew and is

$$\Delta Q_{n-lin} = \Delta Q_{slew}(V_{in}) - \Delta Q_{slew}(0) \tag{8}$$

in case of slewing.

The error becomes strongly non-linear when the slewing period becomes a significant fraction of the injection phase and depends on design parameters and clock frequency. Moreover, the transition from "off" to "on" determined by switches made by MOS transistors smooth the waveforms and reduces the peak value of the virtual ground swing. The behavior, studied at the transistor simulation level, gives rise to the

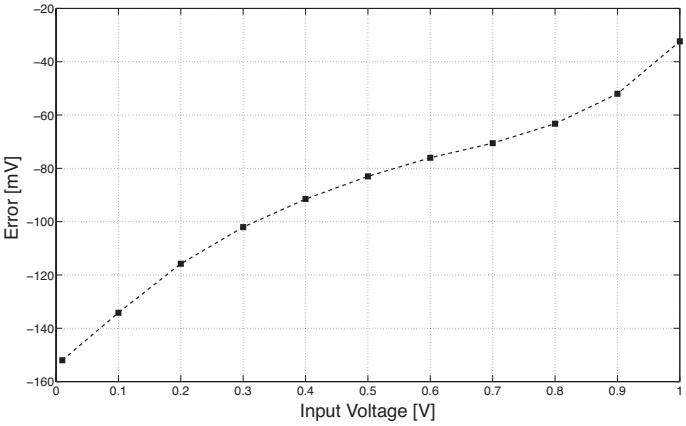

Fig. 3. Simulated error as a function of the input voltage.

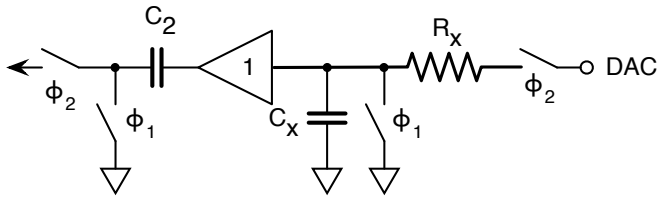

Fig. 4. Scheme of the DAC with controlled rise time.

non-linear error as a function of V_{in} of Fig. 3, obtained with f_s = 100 MHz, g_m = 250 μS, I_{SR} = 50 μA, $C_1 = C_2$ = 0.5 pF, C_L = 1 pF, R_{switch} = 100 Ω, and $V_{DAC} = -1$ V. The error is calculated as the difference at the end of the injection between waveform with infinite and finite slew-rate. For negative values of the input voltage, the behavior is symmetrical.

III. Design Solutions

The use of a SC-DAC limits the error due to the clock jitter, [2], but this simple theory indicates a non-linear error when the op-amp goes in the slewing conditions. Therefore, a generic design guideline is to avoid slewing even if this is obtained at the expenses of a reduction of the op-amp bandwidth.

To overcome the above drawbacks, we propose and discuss three design methods: the use of an attenuating capacitance loading the virtual ground, the use of a DAC with controlled rise-time and a the use of a multi-rate DAC.

A. Virtual ground attenuating capacitance

The use of an additional capacitance, C_a, loading the virtual ground determines an immediate sharing of the charge on C_2. The voltage across the capacitors becomes $V_{DAC}C_2/(C_2 + C_a)$. Since in (1) we have to replace C_2 with $C_2 + C_a$, the attenuation factor α becomes $C_2/[C_2 + C_a + C_1C_L/(C_1 + C_L)]$. If $C_1 = C_2 = C_L$ and $C_a = C_2$, the swing of the virtual ground voltage goes from $0.66\,V_{DAC}$ down to $0.4\,V_{DAC}$. The cost is an increase of the time constant of the successive transient, but the distortion caused by the slew-rate limit significantly reduces.

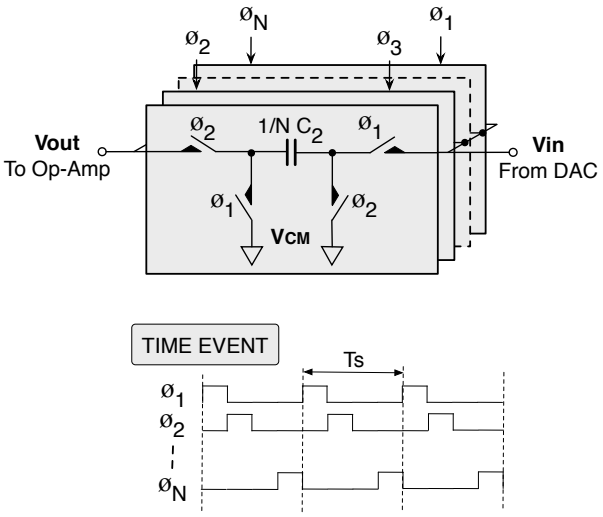

Fig. 6. Scheme of the multi-rate DAC.

B. DAC with controlled rise-time

Fig. 4 uses a switched capacitor injecting structure with the voltage at the right terminal of C_2 that rises exponentially with time constant controlled by the R_xC_x network. Smoothing the rising edge of the DAC voltage limits the current delivered to the virtual ground by the SC-DAC. This favors better linearity because the operational amplifier remains in slewing conditions for a shorter portion of the injecting phase, Φ_2.

Fig. 5 shows the simulated error, calculated with the same parameters used for Fig. 3, as a function of the input voltage value. The used R_xC_x is $T_S/20$. The achieved result is better than Fig. 3 (four times lower), but the error is still non-linear because the op-amp slewing is limited, but not fully avoided.

C. Multi-rate DAC

The multi-rate approach, [5], in the SC-DAC consists in injecting the foreseen charge in N equal time slots within a single sampling period, as conceptually shown in Fig. 6. Since

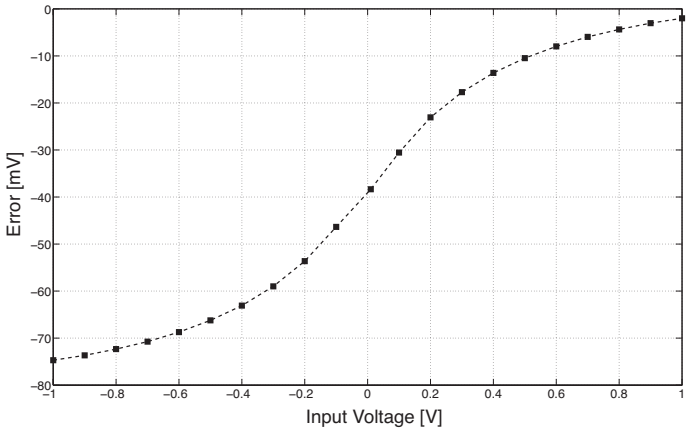

Fig. 5. Simulated error as a function of the input voltage.

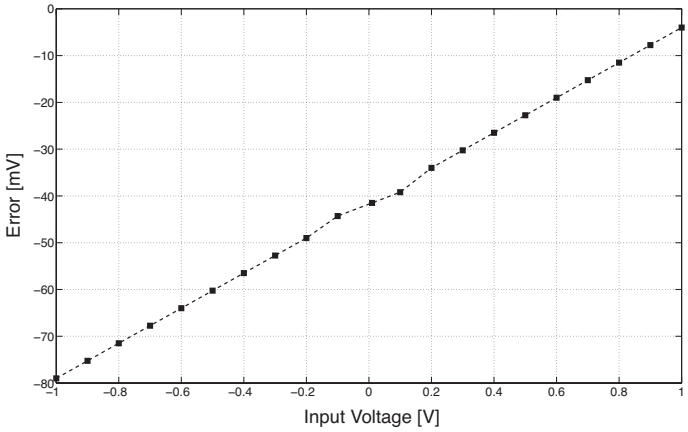

Fig. 7. Simulated error of the multi-rate DAC (4 injections).

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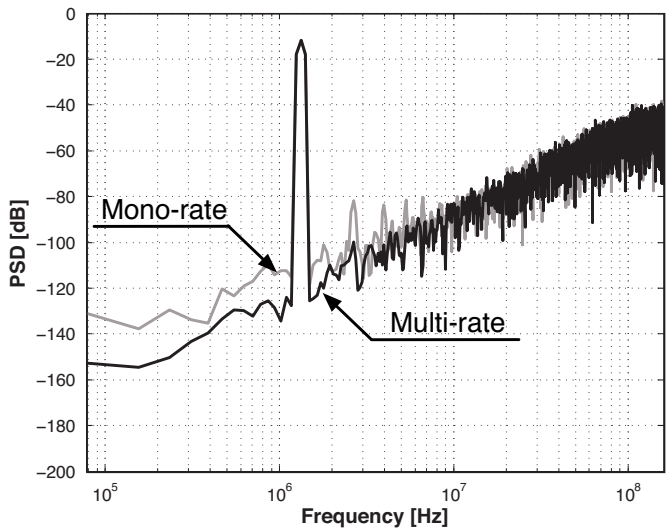

Fig. 8. Simulated output spectrum of the second order ΣΔ modulator. FFT points = 4096.

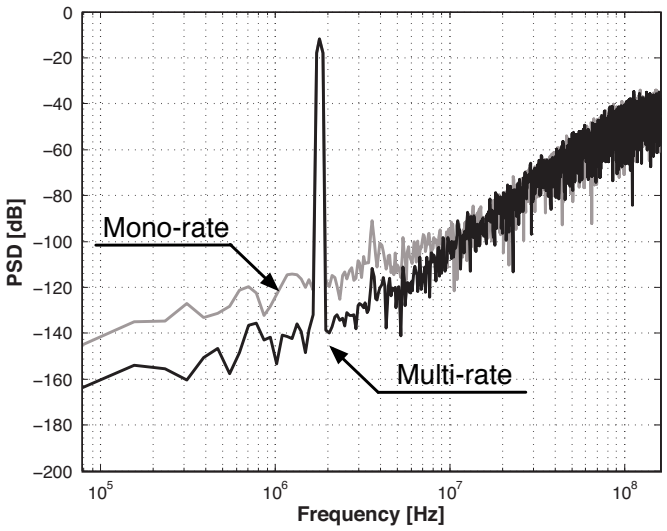

Fig. 9. Simulated output spectrum of the third order ΣΔ modulator. FFT points = 4096.

the injecting capacitor is C_2/N, replacing this value in (1) leads to a strong reduction of the virtual ground swing. Depending on the op-amp performance, it is possible to choose the number of injections that keep the op-amp off of slewing. The optimum number of injections depends on the DAC signal and available op-amp overdrive voltage. The number of required injections can dynamically diminish if the DAC is multi-bit.

Fig. 7 shows the simulated error, calculated with the same parameters used for Fig. 3 (but with double transconductance), as a function of the input voltage. The simulation uses a number of injections equal to 4. The non-linearity is significantly reduced. The reasonable linear error can be compensated for by trimming the value of the DAC capacitance.

IV. Comparing Single-rate and Multi-Rate DACs

To evaluate and compare mono and multi-rate SC-DAC performance, the two approaches have been simulated at behavioral level with a second and a third order CT ΣΔ modulator. The DAC uses 3 bit.

Fig. 8 shows the spectrum for the second order modulator. The sampling frequency is 320 MHz and the oversampling ratio (OSR) is 16. The input signal is 1.32 MHz with -4 dB_{FS} amplitude. In the mono-rate case, a slew-rate as large as 140 V/μs causes harmonic distortion tones. The simulated signal-to-noise distortion ratio (SNDR) is 55.7 dB. With a 4 injections multi-rate DAC, harmonic tones disappear and the simulated SNDR improves by 6 dB.

Fig. 9 plots the output spectrum of the third order modulator. The sampling frequency and the OSR are the same of the second order case. The input frequency is 1.79 MHz at -4 dB_{FS}. The mono-rate solution leads to a SNDR of 70.4 dB while the multi-rate approach with 4 injections gives 78.8 dB.

The use of the control of the DAC rise time as described in Fig. (4) further improves the spectrum and with a time constant $R_x C_x > 0.1/f_{ck}$ the tones completely disappear.

V. Conclusions

The critical study of hybrid continuous time ΣΔ modulators with SC feedback DAC identified the key limit that causes harmonic distortion and SNDR degradation. The use of a multi-rate architecture and a DAC with controlled rise time completely eliminate the limit. The cost is a possible gain error that can be easily corrected by trimming the input resistance or the value of the capacitance of the SC-DAC.

Acknowledgment

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References

[1] J.A. Cherry and W.M. Snelgrove "Continuous-Time Delta-Sigma Modulators for High-Speed A/D Conversion", Kluwer Academic Pub., 1999.

[2] M. Ortmanns, F. Gerfers, and Y. Manolis "A ContinuousTime ΣΔ Modulator with Reduced Sensitivity to Clock Jitter Through SCR Feedback", *IEEE Transactions on Circuits and Systems-I*, vol. 52, no.5, pp. 875884, May 2005.

[3] R.H.M. van Veldhoven, "A Triple-Mode Continuous-Time ΣΔ Modulator with Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver *IEEE J. Solid-State Circuits*, vol. 38,no. 12, pp. 2069-2076, Dec. 2003.

[4] M. Ortmanns, F. Gerfers, and Y. Manolis, "Increased Jitter Sensitivity in Continuous and Discrete Time ΣΔ Modulators Due to Finite Op-Amp Settling Speed *Proc. of IEEE International Symposium on circuits and Systems (ISCAS)*, pp. 22432246, May 2005.

[5] F. Colodro and A. Torralba, "Multirate Single-Bit ΣΔ Modulators *IEEE Transactions on Circuits and Systems-II*, vol. 49, no. 9, pp. 629634, Sept. 2002.