

O. Belotti, A. Pena Perez, F. Maloberti: "**Oversampling Enhancement in Sigma Delta Modulators**"; 7th IEEE Conference on Ph.D. Research in Microelectronics and Electronics, PRIME 2011, Madonna di Campiglio, 3-7 July 2011, pp. 241-244.

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Oversampling Enhancement in Sigma Delta Modulators

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Abstract—A method that virtually double the oversampling ratio of a second order sigma-delta ($\Sigma\Delta$) modulator is described. Accounting for a limited cost, the resolution increases by about 2-bit and power just increases by few percents. Therefore, the FoM diminishes by a factor close to 3.5. Simulation at the behavioral level of the proposed method verifies the operation. Circuit level schemes indicates that the architecture does not requires higher op-amp bandwidth. The method can be used with multi-bit quantizer without requiring additional efforts for the DEM.

Index Terms— $\Sigma\Delta$, oversampling, quantization.

I. INTRODUCTION

Data converters for portable communications must generate medium resolutions (in the range 10-12 bit) but must consume very low power. The parameter that measure the power effectiveness is the Figure of Merit, defined by

$$FoM = \frac{P}{2^{ENOB} 2f_B} \quad (1)$$

where P is the power, $ENOB$ is the equivalent number of bit and f_B is the signal band.

State-of-the-art $\Sigma\Delta$ modulators achieve FoMs lower than $0.2 pJ/conv - lev$ but further reductions of the power level is increasingly required because of the needs of autonomous systems.

The methods that gives rise to optimal power consumption operate on three parameters: order of the modulator, oversampling ratio and number of bit of the quantizer [1]. The choice is typically for second order schemes (unless higher order are obtained with two op-amps), low oversampling and medium-high number of bit. The latter parameter depends on two factors: the power consumption that increases exponentially with the resolution and the number of unity elements that the DEM must average [2]. A common choice is to use a 3-bit quantizer but for medium resolution even 4-bit quantizer is a good choice.

This paper uses as starting prototype a second order modulator with 3-bit quantizer. However, more bit are also usable with the proposed method. Since the described technique virtually doubles the oversampling ratio (OSR) the scheme operates with a given clock frequency but the output digital data is at a double rate. The result, like the time-interleaved schemes reported in [3] and [4], gives rise, ideally to 2.5 extra bit. The benefit, as shown in the following sections, is fully granted

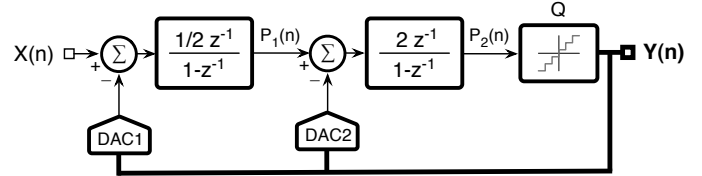


Fig. 1. Conventional second-order $\Sigma\Delta$ modulator.

with an analog solution. A digital realization loses 0.5 bit but requires less additional power.

The following section describes the oversampling enhancement concept, Section 3 presents the behavioral implementation and shows simulation results. Section 4 discusses circuit implementation; the last Section gives some conclusions.

II. OVERSAMPLING ENHANCEMENT

Increasing the oversampling ratio means using more samples of the analog input signal. There are two possibilities, using a faster sampling rate or interpolating the input signal with zero or held replica of the input. Interpolation is common with digital signal but not used for analog. This paper supposes to use an interpolation by 2 to enhance the OSR by 2.

Fig. 1 shows the second order prototype. It uses two delayed integrators with gain 1/2 and 2 for the first and the second stage respectively. The choice accommodates half clock period for the settling of the two integrators, enables half clock period for the flash and the remaining half for DEM and D/A conversion.

The time-domain analysis of the modulator yields, for the first integrator

$$P_1(n+1) = P_1(n) + \frac{1}{2} [X(n) - Y(n)] \quad (2)$$

$$P_1(n+2) = P_1(n) + \frac{1}{2} [X(n) + X(n+1) - Y(n) - Y(n+1)]; \quad (3)$$

where n is supposed an even number. For the second integrator, it results

$$P_2(n+1) = P_2(n) + 2 [P_1(n) - Y(n)] \quad (4)$$

$$P_2(n+2) = P_2(n) + 2 [P_1(n) + P_1(n+1) - Y(n) - Y(n+1)] \quad (5)$$

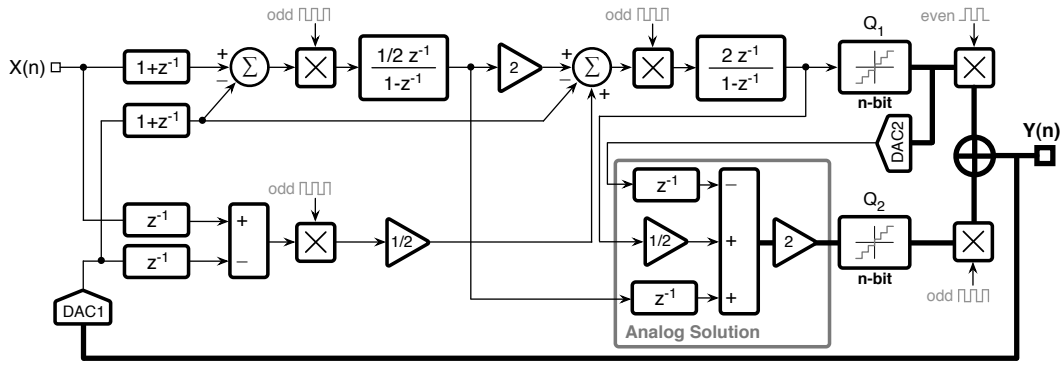


Fig. 2. Second-order $\Sigma\Delta$ modulator with analog oversampling enhancement.

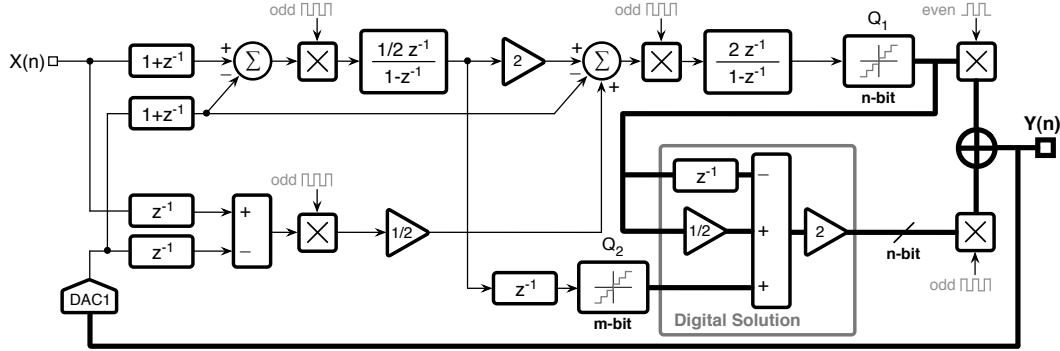


Fig. 3. Second-order $\Sigma\Delta$ modulator with digital virtual oversampling enhancement.

therefore, the output of the first integrator at even times is the output at the previous even time plus the input minus the modulator output passed through the z-transfer function $(1 + z^{-1})$. Supposing that $X(n) = X(n+1)$ the input term is just twice the input at even times. The output of the second integrator at even times is given by the previous even plus output of first integrator minus the output passed, as before, through the z-transfer function $(1 + z^{-1})$.

Similarly, we can write equations that describe the output of integrators at odd times (again we suppose n an even number)

$$P_1(n) = P_1(n-1) + \frac{1}{2} [X(n-1) - Y(n-1)] \quad (6)$$

$$P_1(n+1) = P_1(n-1) + \frac{1}{2} [X(n-1) + X(n) - Y(n-1) - Y(n)] \quad (7)$$

and, for the second integrator

$$P_2(n) = P_2(n-1) + 2 [P_1(n-1) - Y(n-1)] \quad (8)$$

$$P_2(n+1) = P_2(n-1) + 2 [P_1(n-1) + P_1(n) - Y(n-1) - Y(n)]. \quad (9)$$

Supposing again that $X(n) = X(n+1)$ the input term uses one of the equal input pair and the previous one. Therefore, even if almost equivalent, when representing even samples the system looks ahead. When representing odd samples, the system recovers for the sample left behind.

The direct translation of the above equations is given by the analog implementation of Fig. 2. The inputs of the first integrator are the actual inputs plus the recovery term that gives rise to the analog and DAC input multiplied by $(1 + z^{-1})$ as equation (3) describes. The output of the first integrator is then available for two clock periods. The output of the second integrator is also available from even times (injection at $n + 1$ times) and lasts for two clock periods. It as prescribed by equation (5) is $P_2(n)$ added with twice $P_1(n) + P_1(n+1) = 2P_1(n) + 1/2 [X(n) - Y(n)]$ and subtracted from twice $Y(n) + Y(n+1)$. The quantization of the output of the second integrator gives the digital output at even times. The output at odd times must be predicted.

The circuit inside the block “Analog Solution” generates the next odd signal at the output of the second integrator as defined by equation (9). The block requires additions and subtractions that can be performed with a passive network. However, the operation must occur after the even quantization (Q_1). This requires to borrow a significant fraction of the full period.

There are other possible analog architectures that anticipate the generation of the even signal. The cost of the benefit is an extra op-amp that limits the power benefit [3].

III. DIGITAL VIRTUAL OVERSAMPLING

The problem of the cascade of two quantizer and the need of using an extra DAC, as illustrated by Fig. 2, is resolved by the digital solution of Fig. 3. The scheme is formally the

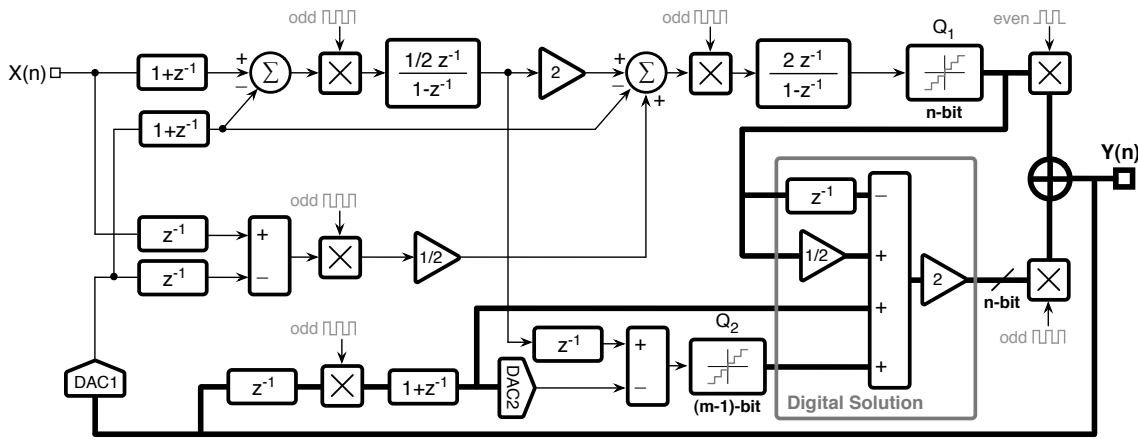


Fig. 4. Swing reduction of Q_2 in the second-order $\Sigma\Delta$ modulator of Fig. 3.

same but the “Digital Solution” block replaces the “Analog Solution” block by the use of a second quantizer (Q_2) that converts the output of the first integrator. The foreseen delay of the analog scheme provides the time needed for the A/D conversion. Moreover, the digital output replaces the analog output of the second integrator.

The given solution is a trade-off between many possible schemes. Indeed the use of higher resolution in the digital paths that replace the analog signals would improve the result. The scheme of Fig. 3 uses the same number of bit, n , for the P_2 path and $m \geq n$ for the P_1 path.

The architecture of Fig. 3 can be improved because the signals at relevant nodes of the quantizer are the input plus shaped quantization noise. For a multi-bit scheme the noise term is small and because of oversampling there is some correlation between successive input samples [5]. The proposed scheme of Fig. 4 exploits that property. The input of Q_2 is the signal P_1 subtracted to a suitable processing of the digital output. The result is that the input range of the quantizer is halved.

Therefore, even if the quantization step remains the same the equivalent number of bit diminishes by one. Fig. 5 shows the output P_1 and the input of Q_2 with a -3 dB_{FS} signal and frequency at the limit of the band ($OSR = 16$).

The architecture of Fig. 4 has been simulated at the behavioral level. As shown in Fig. 6 the conventional $\Sigma\Delta$ modulator of Fig. 1 with $OSR = 16$ and 3-bit quantizer achieves a $SNR = 62.08\text{ dB}$. The proposed scheme of Fig. 4 with digital OSR enhancement grants about 12 dB equivalent to 2-bit. The result is for a 4-bit Q_2 quantizer. The 0.5-bit loss respect to the ideal 2.5-bit (determined by a doubling of the OSR) is because of the performed digital approximation.

Fig. 7 shows the SNR at different input amplitudes and various Q_2 resolutions. Notice that the use of a 3-bit quantizer determines only 9 dB improvement; the use of 4-bit grants about 12 dB with a limited additional benefit for higher resolution. The use of 4-bit on both P_1 and P_2 paths gives rise to about an overall 13.5 dB benefit.

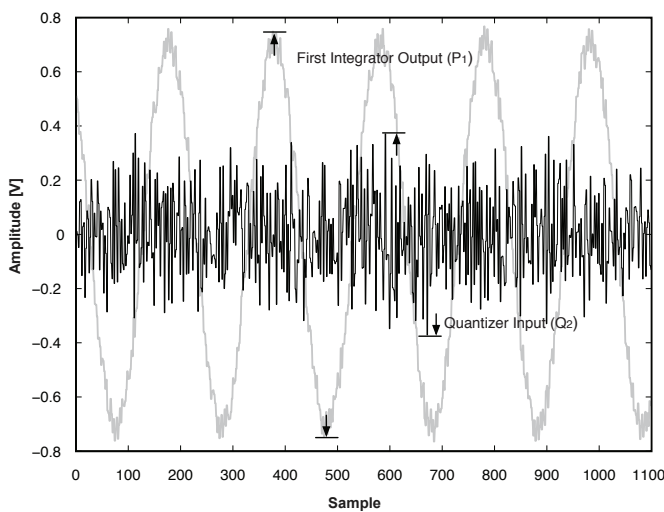


Fig. 5. First integrator output signal and input signal of quantizer Q_2 .

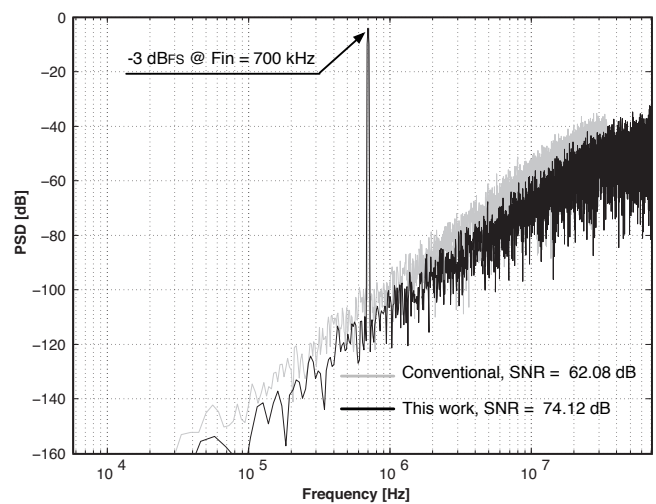


Fig. 6. Simulated power spectrum density. FFT points=12288.

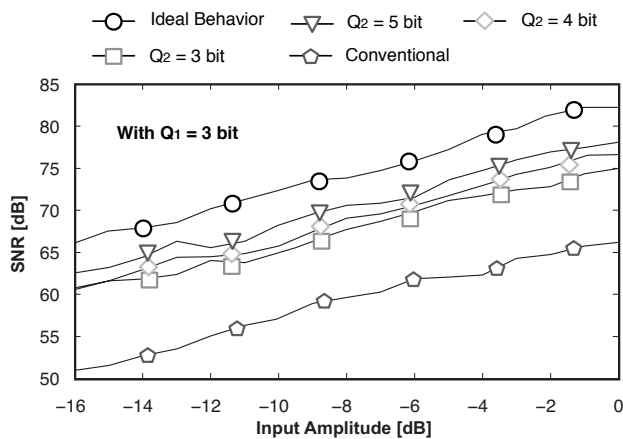


Fig. 7. Simulated SNR vs input amplitude.

IV. CIRCUIT IMPLEMENTATION

The implementation of the scheme of Fig. 4 must realize an additional transfer functions equal to $(1 + z^{-1})$ at the input of the first integrator. Moreover the input of the second integrator needs an equal transfer function on the digital path, added to the multiplication by two P_1 plus an extra term given by the combination of an analog and digital converted term.

The design goal is to realize the functions with the minimum number of unity capacitors and to favor, when necessary, a proper dynamic matching of unity elements. For the optimal circuit implementation it is worth nothing that:

- The outputs of the two integrators last for two clock periods starting from the odd times.
- The flash converters generates the digital signals with short delay. The first is the even output followed by the odd by the delay established by the digital processing of the digital section. In practical cases the delay is a small fraction of the clock period.
- The input signals are possibly the result of an interpolation by two. In this case the even value equals to the previous odd.

The above point suggest to use, in fully differential implementation, input structures like the ones of Fig. 8. The one on Fig. 8(a) can be used for the input signal. The driving phases are depicted in Fig. 8(c). Phase Φ_1 and Φ_2 last for two entire clock periods thus ensuring the longest time for the input injection and settling of op-amps. The scheme operates like a biquad parasitic insensitive SC structure. During phase Φ_1 , the top capacitor injects the signal at odd times being pre-charged to the inverse of the input at the even times. The same does the bottom capacitor during phase Φ_2 .

The scheme of Fig. 8(b) serves for the injection of the DAC signals. The capacitors are pre-charged at the proper value with a phase that is shorter than the one used for the injection. The reason is that passive charging is faster than the virtual ground injection being only limited by the on-resistance of the switches. Similar strategies are used for the injection of signals at the input of the second integrator.

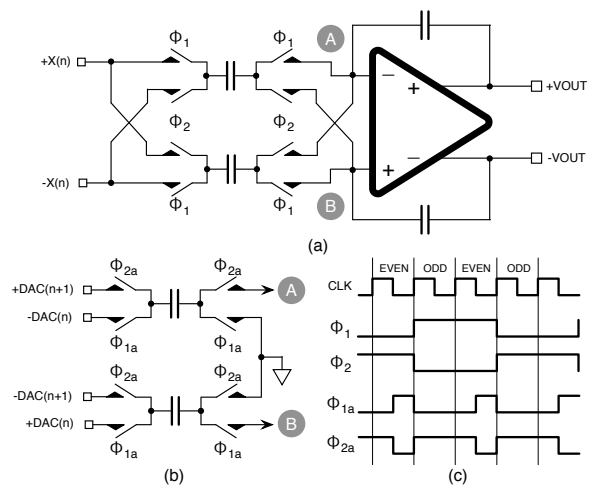


Fig. 8. Possible fully differential SC implementation.

An interesting feature of the solution proposed in Fig. 8 is that for multi-bit DAC the switched capacitor is divided into unity elements. They are used for both conversion of the digital signal of the even and the odd phases. This gives rise to the two conversions without using twice unity elements. Moreover, if DEM is needed the circuit must use two n -bit DEM, one for the even conversion, the other for the odd conversion instead than a more cumbersome $(n + 1)$ DEM.

V. CONCLUSIONS

A second order $\Sigma\Delta$ modulator with digital virtual oversampling enhancement has been described. The proposed architecture achieves an increased resolution of about 2-bit respect to the conventional solution. The digital approximation loses 0.5 bit respect to the ideal behavior but requires less additional power and avoids the necessity of an extra op-amp. The fully differential switched-capacitor implementation grants the realization of the additional transfer function $(1 + z^{-1})$ in both integrators, with a minimum number of unity capacitors. Furthermore benefits the DEM operation without using twice unity elements.

ACKNOWLEDGMENT

The authors would like to thank FIRB, Italian National Program #RBAP06L4S5 for partial economical support.

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