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An Analog Readout Circuit with Offset Calibration for Cantiliver-based DNA Detection

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Abstract—In this paper a readout circuit for label-free DNA detection based on piezo-resistive MEMS cantilevers is presented. The circuit is designed to have high sensitivity and a precise calibration block in order to deal with possible large variation of the cantilever resistance due to technological mismatch effects. The readout channel has been electrically tested showing, as preliminary results, a total differential dynamic range of 35dB with 15μV as best input resolution, a static offset compensation of about 78dB and a common-mode rejection of about 58dB with about 2.2% of linearity, which demonstrates the suitability of the proposed architecture for the target application. The chip consumes about 10mW from a 3.3V power supply, while the area occupation is of about 1.05mm² (pad excluded).

I. INTRODUCTION

The growing of new sophisticated technique of DNA typing can provide new genomic tests for improving the diagnosis of diseases with a genetic pattern like rheumatoid arthritis and multiple sclerosis. In this context the need to use compact systems able to detect a certain number of DNA sequences in a fast way, brought to the idea to realize Lab-On-Chip (LOC) instruments where detection and custom readout circuit are integrated onto the same microsystem. Particularly interesting are those systems able to autonomously perform DNA detection starting directly from biological samples such as blood or saliva thanks to microfluidics, sample handling, and proper biological processing capabilities. DNA detection can be performed using different techniques. Because of its robustness, the optical measurements based on fluorescence detection is one of the most used approach. On the other hand a label-free technique represents a newsworthy alternative thanks to their high parallelism, which potentially allows to perform multiple detections on the same chip thus introducing redundancy and complementary measurements. The proposed label-free approach uses a static piezo-resistive micro-cantilevers coated with proper single strand DNA probes for selectively binding a specific DNA sequence (hybridization过程). During the hybridization the cantilever is mechanically deflected [1] because of the differential stress between the top and the bottom surfaces induced by the interaction with the target DNA (see Figure 1). The equivalent resistance variation around the equilibrium point is expected to be very small [2-3] if compared with the unavoidable resistance mismatch due to technological process variations. In particular, if the detection of Single Nucleotide Polymorphisms (SNPs) is required, the resulting resistance variation is in the order of few ppm, while mismatches and mechanical imperfections can easily provide a resistance deviation of some percent. As a consequence the proposed readout circuit has been designed to achieve a high sensitivity, in order to measure very small variation of resistance around a defined working point, and also the capability to adjust the range of operation in the presence of a large input offset. Moreover, for the proposed application the goal of the circuit is to detect if hybridization occurred or not giving, as a final output, a binary value.

Figure 1: MEMS cantilever for DNA detection.

Looking at the state of the art, many examples of very accurate readout circuits for resistive sensors have been proposed for a variety of applications [4-7]. The approach used in [4-5] is based on resistance-to-period conversion obtained by charging and discharging an integration capacitor by the current flowing into the resistance to be detected. Both works allow to cover a wide range of resistance values (more than three decades) reaching a best accuracy of 0.5%, which is not suitable for the present application. The work presented in...
The designed piezo-resistive MEMS cantilevers are organized in a 4-terminal Wheatstone bridge, consisting of a couple of bulk resistors, to reject thermal effects, plus a couple of beams for implementing a differential measurement where a reference beam is used to reject all non-specific interaction with the sample. The cantilever piezo-resistance $R_c$ can then be represented by the combination of four components: the baseline $R_{bs}$, which is the nominal value of the resistance; the deviation from the baseline $\Delta R_{cb}$ due to process parameters variation of the technology; the variation $\Delta R_{cd}$ due to mechanical deflection of the beam measurable also under static condition; and the biological-induced signal $\Delta R_{cs}$ due to the hybridization process:

$$R_c = R_{cb} \pm \Delta R_{cb} \pm \Delta R_{cd} \pm \Delta R_{cs}$$

Despite the last contribution, all these electrical and mechanical mismatches introduce an equivalent offset detectable at the output of the bridge which can be estimated three order of magnitude greater than the expected useful signal. In order to deal with the undesired imbalance of the bridge because of detector non-idealities the proposed circuit implements a proper offset calibration procedure before the hybridization step. In particular a single measurement is divided in three phases: 1) a two steps calibration procedure executed before the hybridization process; 2) a successive measurement for the residual offset $M_{off}$ before hybridization; 3) a signal measurement after hybridization $M_{sig}$. The final value of the measurement will be computed as the difference $M_{sig} - M_{off}$.

III. CIRCUIT IMPLEMENTATION

A simplified circuit schematic of the read out circuit is shown in Figure 2. The channel consists of three main functional blocks: a first transconductance stage with coarse calibration circuit (CAL1) able to balance the bridge and bias the circuit, followed by a programmable current adder block and a final integrator stage for signal accumulation with a sampling and hold capability. As shown in Figure 2 the readout circuit can be connected only to a single detector even if, in perspective, an additional block will be further implemented for multiplexing more inputs coming from an array of multiple detectors.

This first coarse calibration has to assure equal currents flowing into the two circuit branches, minimizing in this way the offset contribution due to the bridge mismatch and opamp amplifiers Op1-Op4 input offsets. In particular, being current $I_A$ mirrored and subtracted to $I_B$, the voltage output, as a result of the current integration, should be as close as possible to $V_{ref}$ after the coarse calibration. The relationship between $V_{DAC1}$ (and DAC2) and the related current variation is obviously done by dividing the voltage drop $\Delta V_A (\Delta V_B)$ by the value of the integrated resistance $R_A (R_B)$. Because of the high gain introduced by the first stage and because of the limited resolution of this first calibration, an optimal current matching is not possible using CAL1, resulting in a positive or negative voltage ramp at the output. In order to improve the calibration procedure, a programmable current mirror is used for finely tuning the output current $I_A$ and better equalling $I_A$ with $I_B$, avoiding the saturation of the integrator.

This second finer calibration is then able to better compensate the input offset coming from the bridge, partially resolved by the coarse calibration, and also to reduce possible electronic mismatch due to the mirror circuit and possible intrinsic offset of Op3 and Op4. The programmability of the mirror circuit is implemented by forcing M5 and M6 in triode region by means of $V_{DAC_M3}$ and $V_{DAC_M4}$ through transistor M3-M4. For little changes of $V_{DAC_M3}$ an approximately linear current variation is expected at the output. Considering M5 and M6 in triode
region and approximating \( V_{DAC} = V_{DAC\_M3} - V_{T3} \) (same considerations can be applied also to \( V_{DAC\_M4} = V_{T4} \)), the output current \( I'_{A} \) can be expressed by the following relationship:

\[
I'_{A} = I_{A} \left( \frac{V_{DAC\_M4} - V_{T4}}{V_{DAC\_M3} - V_{T3}} \right) = I_{A} k
\]

(2)

This means that once the value of \( V_{DAC\_M3} \) is fixed, defining the slope of the current variation, \( I'_{A} \) can be linearly modified as a function of \( V_{DAC\_M4} \). The family of curves of Figure 4 represents a simulation of the current \( I_{OUT} = I_{B} - I'_{A} \) when \( I_{A} = I_{B} \) as a function of \( V_{DAC\_M4} \) for different values of \( V_{DAC\_M3} \). As equation (2) states, \( V_{DAC\_M4} \) influences the slope of the curves, while \( V_{DAC\_M4} \) determines an approximately linear modification of the current. Depending on the value of \( V_{DAC\_M3} \), the minimum current step can vary from 2\( \mu \)A to really small current modification which depends on the channel-length modulation effect \( \lambda \). Considering also the contribution due to the coarse calibration, it is possible to write an approximated relationship between \( I_{OUT} \) and the values imposed by the DACs:

\[
I_{OUT} = I_{B} - I'_{A} = \frac{V_{DAC\_B} - V_{B}}{R_{B}} - \frac{(V_{DAC\_A} - V_{A})}{R_{A}} \left( \frac{V_{DAC\_M4} - V_{T4}}{V_{DAC\_M3} - V_{T3}} \right)
\]

Noise-tran simulations and input referred noise calculation reveal that overall noise is dominated by \( 1/f \) contribution mainly introduced by Op3 and Op4 while Op1 and Op2 noise are filtered out by an external capacitance. For this reason short integration time are used (typically in the order of \( T_{int}=20\mu s \)). Moreover, even if the hybridization is a quite long process (few seconds), short integration time for signal accumulation is desirable in order to execute multiple acquisitions and reducing power dissipation on the bridge. Using a 1% of duty cycle, this technique allows to bias the channel and then electrically stimulating the circuit with a programmable voltage generator. In order to properly stimulate the circuit with a small voltage step (in the order of \( 10 \mu V \)), a manually-selectable RF attenuator from 0 to 120\( dB \) has been used. As described in Section II the measurement has been performed by firstly calibrating the channel and then electrically stimulating the circuit with a voltage ramp and acquiring a certain number of samples in order to measure mean value and standard deviation for each input voltage step. Coarse and fine calibrations need a proper procedure in order to optimize the circuit performance. In particular coarse calibration is critical for defining the bias condition of the circuit. The two DACs (\( DAC_1 \) and \( DAC_2 \)) are programmed by means an up counter, set to the minimum value under reset, through two independent input clocks. The coarse calibration procedure can be automatically done by acquiring \( V_{A} \) and \( V_{B} \) and imposing \( V'_{DAC\_A} = V_{A} + 3mV \) and \( V'_{DAC\_B} = V_{B} + 3mV \). The procedure firstly imposes \( V_{DAC\_B} = V'_{DAC\_B} \) forcing in this way \( I_{OUT}=I_{B} \) and, consequently, a negative voltage ramp on \( V_{out} \). As second step, the coarse calibration tries to impose \( V_{DAC\_A} = V'_{DAC\_A} \) so that \( I_{OUT}=0 \) and \( V_{out}=V_{ref} \). Because of the high gain of the first stage and the resolution of the coarse calibration, a perfect current balancing will be difficult to reach. The fine calibration helps the circuit to find this condition by tuning the current \( I'_{A} \). Also in this case \( DAC_3 \) and \( DAC_4 \) are programmed by two independent down-counters set to the maximum allowable value during the reset condition. The two different calibration modalities have been generated. The final sensitivity of the circuit can be computed by considering the following formula:

\[
S = \frac{(\Delta R)}{(R^2)} \cdot \frac{V_s}{G \cdot T_{int}} = \frac{V_s \cdot T_{int} \cdot 50 \cdot \frac{V}{s}}{ppm}
\]

where \( V_s \) is the voltage supply of the bridge, \( G \) is the circuit gain and ppm is the resistance variation expressed in ppm. Considering \( V_s=3V \), \( T_{int}=100\mu s \) and 10ppm of resistance variation, the expected output voltage will be about 150mV.

The microphotograph of the circuit, implemented using a CMOS 0.35\( \mu m \) technology, is shown in Figure 5 where the four calibration circuits are highlighted together with the integrator and the input stage. The area of the circuit is of about 1.3x0.8\( mm^2 \) pad excluded.
evaluated in term of resolution, by measuring the output voltage variation caused by the minimum voltage step imposed by the DAC. The effect of the calibration is to create an artificial input offset able to compensate the bridge unbalancing. The input referred calibration resolution will be computed by dividing the output voltage by the circuit gain. The measurement of the effect of the fine calibration on Vout is shown in Figure 6, where an integration time of 50μs has been set for the experiment. In the two plotted curves the voltage $V_{DAC,M4}$ is swept forcing M5-M6 in triode or in saturation region. In particular Figure 6 shows that in linear region ($V_{DAC,M4}=V_{DAC,M3}=0.45V$) the achievable resolution, expressed in term of equivalent input voltage, is of about 50μV, while in saturation ($V_{DAC,M4}=V_{DAC,M3}=1V$) can reach the value of about 6μV. The coarse calibration instead is in the order of 1mV, but can be improved by shrinking the working range of the DAC1-DAC2.

Figure 6: Vout variation depending on the fine calibration input values.

Thanks to the calibration procedure, the circuit is able to compensate an artificial input voltage offset of about ±200mV which corresponds to an equivalent resistance variation of more than 10% when the bridge is biased with a 3V power supply, perfectly matching the target specifications. Because of the noise measured at the output of the circuit, caused by the high circuit sensitivity, the resulting differential dynamic range has been estimated to be about 34dB. This is enough for obtaining a good discrimination between the situation of DNA hybridization with respect to the absence of DNA attached on the cantilever surface. In perspective, dynamic range can be extended exploiting the static calibration and a proper external logic for dynamically compensate the input signal variation. In Figure 7 are plotted five different curves obtained by superimposing $\Delta V_{in}$ to an additional offset approximately null (central curve), and of about ±100mV and ±200mV respectively. During the experiment the circuit has been excited using a voltage ramp $\Delta V_{in}$ with a step of about 3μV (obtained imposing an attenuation of -50dB) and integrating the output current for 30μs. Each point of the curve is the result of the average of 1000 samples, resulting in an acquisition time of about 40ms. The calibration procedure, applied before the voltage ramp, allows to successful compensate the input offset avoiding the saturation of the integrator. Best achieved input resolution is measured below 15μV, the linearity of the traced curves is calculated to be about 2.2% over the entire range while the gain variation is of about 0.15% under the different bias conditions. Differential offset rejection is estimated about 78dB. Common-mode offset rejection depends on the input range allowable for the circuit (which can theoretically vary from 2.8V to 1.1V) resulting in about 58dB.

![Figure 7: Vout variation after calibration for a maximum of ±200mV as differential input offset.](image)

V. CONCLUSIONS

An analog high-sensitivity readout channel for piezoresistive cantilever-based detection has been described. The circuit shows the ability to compensate up to 200mV of offset variation with a best input sensitivity of 15μV (see Table 1) showing the suitability of the circuit for the target application.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
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<tbody>
<tr>
<td>Technology</td>
<td>CMOS 0.35μm</td>
</tr>
<tr>
<td>Occupational Area</td>
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<tr>
<td>Power Consumption</td>
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<td>Coarse Calibration Resolution</td>
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<tr>
<td>Fine Calibration Resolution</td>
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<td>Best Input Resolution</td>
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<td>Differential-mode offset compens</td>
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<td>Common-mode offset compens</td>
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REFERENCES