A VERSATILE CMOS DAC-DRIVER FOR RESISTIVE ACTUATORS

F. Maloberti, G. Polito*, F. Tagliani, G. Torelli

Department of Electronics, University of Pavia,
Via Abbiatograsso 209 - 27100 Pavia - Italy
* Marelli Autronica , R & D Center,
Corso G. Cesare 328 - 10100 Torino - Italy

SUMMARY

A system for the digital signal processing and the direct driving of a resistive actuator is described. The digital section uses oversampling and linear interpolation techniques to obtain a significant chip area reduction without degrading conversion characteristics. The D/A converter is capable to directly drive a current-controlled resistive actuator providing a satisfactory conversion linearity over the whole output current range. The converter has been developed using a conventional digital 3-μm CMOS technology, so it is particularly flexible and is suited to be integrated in the same chip together with the digital processing section. An application of the proposed technique for the implementation of the display section of a tachometer is presented.

INTRODUCTION

The emergence of powerful digital signal processing capability, together with the high integration level achievable in CMOS integrated circuits, is changing conventional approaches to signal processing. More flexible solutions and, much more important for many applications, a better noise immunity can be achieved with a digital approach. In a number of applications encountered in several fields (e.g. in the automotive one), processing results are required to be used in an analogue form. In some situations, an actuator must be suitably driven. In many cases, even when processing products are not used to control a machine-member but are simply displayed, analogue driving is often necessary as analogue displays using a mechanical pointer are generally preferred to LCD (or similar) digital displays.

Fig. 1 shows the block diagram of the signal processing path followed when the processed information is used to drive an actuator. The input signal, which is normally generated by a sensor, is analogue. It is pre-processed by a simple block (usually an anti-aliasing filter), and then sampled and converted into a digital signal. The linear or nonlinear processing of the signal is performed by a suitable digital network, and the result is converted back into an analogue signal, which is finally provided with the power required to drive the actuator.

In the processing chain of Fig. 1, the analogue interfaces are the most critical elements, as they are the most sensitive to noise and electromagnetic (e.m.) interferences. According to the general trend, these interfaces should be implemented using as simple structures as possible; the required signal-to-noise ratio is achieved by means of an oversampling approach [1], which can be associated to noise shaping techniques. Signal oversampling spreads the power of the noise due to inaccuracies over a wider spectrum, so that a lower amount of noise power falls inside the signal bandwidth [2], [3]. Thus, a relatively low accuracy is required of the A/D and D/A converters. At the extreme limit, data converters with only one bit of resolution (delta or sigma-delta converters) could be used. In this
case, however, in many applications the oversampling factor pushes the operating frequency in the MHz range.

To make a system more reliable and less expensive, the D/A converter should deliver an output signal provided with enough power to directly drive the actuator or an external bipolar power transistor which in turn drives the actuator, therefore the two last blocks of the schematic diagram in Fig. 1 should be reduced to a single element. In this case, of course, the signal power required at the output of the data converter is higher than in conventional applications. By contrast, the conversion accuracy necessary in several applications is generally not very stringent, as it is usually comprised in the range from 7 to 10 bits, with an integral linearity of 1 LSB. The design of D/A converters with the above features ("DAC-drivers") is a specific need of a number of fields, such as automotive and robotic ones.

This paper presents an example of a CMOS integrated system dedicated to the processing and the direct driving of resistive actuators. In order to face the specific aspects of a practical implementation, an actual design problem, i.e. the design of a system for the driving of the crossed coils of a measurement and indication instrument, specifically of a tachometer, is considered.

**SYSTEM DESCRIPTION**

The display section of a mechanical tachometer is made by two fixed crossed coils which are placed orthogonally to each other. The display pointer is fixed to a permanent rotating magnet placed in the area common to the coils. The currents flowing through the coils give rise to two orthogonal strength components acting on the magnet, thus determining the pointer angular deviation. Usually, 270° is the maximum required deviation of the pointer, and ±1° of angular resolution is satisfactory. Therefore, an 8-bit accuracy is necessary in the generation of the coil currents. The typical parasitic series resistance of the coils to be used in such instruments is 250 Ω. The full-scale driving current is 15 to 20 mA, in order to provide enough strength while maintaining a suitable circuit bias.

The schematic diagram of the system proposed to implement the tachometer is shown in Fig. 2. The system input signal consists of a train of pulses generated by a magnetic sensor which detects the rotation of the transmission shaft. The time interval between two successive pulses carries the speed information. This interval is measured and the result is digitally processed to extract the current speed information and make it suited to be displayed by means of a crossed-coil instrument. Not only digital processing allows noise immunity to be improved, thus increasing measurement safety, but also makes it possible to introduce additional features. As an example, to prevent "jitter" in the pointer deviation in the case of a constant speed, an hysteresis is provided in driving the display with the updated information. The updating of the displayed information is also provided with damping to avoid sudden variations in the pointer deviation in response to fast changes in the measured speed; when required, damping can be different in the cases of increasing and decreasing speed.

To obtain a pointer angular deviation which is directly proportional to the value of the variable to be displayed, the two orthogonal components of the strength acting on the rotating magnet of the
instrument have to be proportional to the sine and the cosine, respectively, of the angular deviation to be obtained. The digital word containing the speed value is then transcoded according to the sine and cosine laws to generate two digital words, which in turn are D/A converted to generate the analogue currents which are fed to the two crossed coils. The transcoding according to the required laws is performed by means of two read-only-memories (ROM's). The use of a ROM approach gives a high degree of flexibility in the transcoding law to be realized, allowing changes when a different use of the system is made. For the implementation of a fuel level indicating instrument, for example, the transcoding law can be determined in accordance with the geometrical shape of the fuel tank.

To provide the resolution required by the tachometer, the digital word containing the speed information has 8 bits, so an 8-bit digital processing is performed. In the discussed system, the transcoding 8-bit input, 8-bit output ROM's and the 8-bit D/A converters require a large chip area. The architecture shown in Fig. 2 was used in order to reduce the complexity of the two blocks, while maintaining the required conversion accuracy.

To reduce the ROM size, the digital transcoding according to the sine or cosine law is performed with an $n$-bit input, 8-bit output ROM ($n < 8$). The required resolution is obtained anyway by means of a linear interpolation technique performed at an oversampling rate (block A in Fig. 2). Only the $n$ most significant bits of the digital word are used to perform transcoding. The $8 - n$ least significant bits are iteratively summed at the oversampling rate by means of an accumulator. When a carry is
generated, it is summed to the \( n \)-bit word which is being transcoded, thus giving rise to the word which is actually fed to the ROM input. To make an example, if \( n = 5 \), when the value to be transcoded is 50, the actual sequence of values which are transcoded at a higher rate is 48, 48, 48, 48, 48, 48, 56, 48, 48, 48, 56, 48, a.s.o. Of course, an error results when transcoding is performed with a linear interpolation technique, as the transcoding function is not linear. However, this error has been estimated to be smaller than \( \pm 0.5\% \) and \( \pm 0.15\% \) of full-scale value, respectively, when \( n = 4 \) and \( n = 5 \). Such a small error can be accepted as far as it is smaller or comparable to the quantization error corresponding to the 8-bit conversion, thus leading to a significant reduction in chip area. It is worth pointing out that the same digital word is fed to the input of the two transcoding ROM’s. Therefore, when the described system is integrated in a monolithic chip, the two transcoding functions will be merged into a single ROM, to achieve further area reduction.

To reduce the complexity of the D/A converters, an oversampling approach is followed (blocks B1 and B2). As shown in Fig. 2, oversampling is implemented with a circuit identical to the circuit used to perform the linear interpolation of the word to be transcoded. The oversampling technique used to reduce the number of bits to be D/A converted can be regarded as a first-order sigma-delta modulation [1], [2], [3]. When this technique is followed, a lower resolution is required of the D/A converter. The overall quantization noise power, in fact, is spread over a large frequency band (zero to \( f_s/2 \), where \( f_s \) is the sampling frequency), and the greater part of it falls outside the signal bandwidth and is easily filtered out by the system. In our case, no additional electronic filtering circuit is needed because of the low-pass action of the electromechanical indicating system, which thus ensures a stable position of the pointer (the corner frequency of the system is lower than a few hundreds Hz). The clock frequency used in the sigma-delta modulator must be high enough to prevent acoustic noise, and at the same time it must be low enough to prevent e.m. interferences. A suitable clock frequency can be in the range from some tens to few hundreds kHz. With such an oversampling, a reduction of 3 to 5 bits can be achieved in the resolution required of the D/A converter. The developed system uses two D/A converters with a 5-bit resolution and an 8-bit accuracy.

**D/A CONVERTER**

A schematic diagram of the electrical connection of one tachometer coil is shown in Fig. 3. In automotive applications, a single-voltage power supply \( V_{DD} \) equal to 10 V is generally used.

When current-controlled actuators such as coils are to be driven, current-switched converters [4] are the most suited. In these converters, the output variable is a current which is proportional to a fixed unity-current source \( I_0 \). The proportionality factor is given by the digital value to be converted, and the output current is physically obtained by means of matched replica of the elementary source.

When the actuator is characterized by a non negligible parasitic series resistance and the full-
scale driving current is fairly large, a basic problem to be faced when designing the D/A converter, is to provide the required conversion linearity over the whole output current range. In fact, a significant voltage drop occurs on the actuator’s resistance in the presence of a large output current, therefore the large-signal output resistance of the sources which generate the converter output current, has to be very large with respect to the actuator’s resistance to provide the required conversion linearity. It is easy to estimate that to guarantee an integral linearity of 1 LSB in an N-bit D/A converter, the output resistance of an elementary output current source has to be \( \sim 2^{2N} \) times larger than the actuator’s resistance.

In the case of a display instrument such as a tachometer, the components of the strength acting on the magnet have to be bidirectional, therefore the D/A converter has to be capable to deliver both a positive and a negative output current. In practice, two complementary output sections are provided in the D/A converter, one for the positive output current and the other for the negative output current. When the actuator’s resistance is 250 \( \Omega \) and an accuracy of 7 bits is required for each output section of the converter, the output resistance of the unity current sources has to be larger than 4 M\( \Omega \). To achieve the required high value of output resistance, conventional current sources featuring high output resistance, such as cascode stages, can not be used, as they impose heavy limitations to the output voltage dynamic range due to the fact that the transistors which implement the output current sources have to work in their saturation region. By contrast, a large output voltage dynamic range is required as, when the output current is very large, the output voltage is pushed close to the positive or to the negative supply voltage.

The circuit diagram of the output current sink section of the CMOS D/A converter developed for the proposed system is shown in Fig. 4 [5]. The output current sources are binary-weighted scaled replica of a unity-current source \( I_0 \); the scaling factors are \( 1, 2, ..., 2^{N-1} \) (in our case, \( N = 4 \)). The output current sources are implemented with a single transistor, to allow a very large output voltage dynamic range. Following the current-switching conversion principle, the current delivered to the output is obtained by selectively summing the currents generated by the output sources. The selection is performed by means of switches \( S_0, S_1, ..., S_{N-1} \), in accordance with the N-bit digital word to be converted.

A negative-feedback loop is provided to ensure an optimal matching between the output current sources and a fixed reference current \( I_R \). The bias voltage \( V_B \) drives the output current sources. It is adjusted, depending on the converter output voltage \( V_{OUT} \), so to make a master current \( I_M \) equal to the reference current \( I_R \). In the steady state, the master current \( I_M \) is equal to the difference between currents \( I_2 \) and \( I_3 \), which both are scaled replica of the reference current \( I_R \). By means of a proper size of the used transistors, this difference current is made equal to \( I_R \). The voltage \( V_M \) across the master current source (transistor MM) follows exactly the output voltage \( V_{OUT} \), as the current densities through transistors M1 and M2 are made equal. The selected output current sources work in identical biasing conditions with respect to the master current source, therefore they generate a current which is perfectly matched with the current \( I_R \) regardless of the value of the output voltage \( V_{OUT} \), as long as the transistors of the circuit work in their saturation region. The bias voltage of the current sources, \( V_B \), is controlled by the negative-feedback loop consisting of transistor M2 cascaded with the folded structure made by transistor M3 loaded with the cascaded transistors M4, M5. The open-loop gain of this control loop is in the order of \( (g_{m2}r_o)^2 \), provided that the transistors work in their saturation region, therefore it ensures a very large output resistance of the current sources down to a low value of \( V_{OUT} \), as required in order to provide the required conversion linearity over a large output voltage range. Currents \( I_1 \) and \( I_4 \) are made equal, so they do not affect the converter output current. The contributions to the output current due to mismatches in the control loop biasing currents are minimized by means of a proper design.

The output current source section is exactly alike to the output current sink section shown in Fig. 4, so it ensures the required linearity also in
the second half of the conversion characteristic. The current mirrors between the two sections, as well as the mirrors inside each section, are realized by means of cascode structures to ensure a high precision in mirroring ratios. This is necessary in order to provide the same slope to the conversion characteristics of the two sections, which in turn ensures the required overall conversion linearity.

The described D/A converter was developed in a conventional 3-μm CMOS technology. As pointed out before, the D/A converter needed in the system here proposed for the tachometer application, requires a 5-bit resolution with an 8-bit accuracy (sign included). This can be achieved when the output current sources are implemented using transistors having non minimum length which are biased with a fairly large overdrive voltage and are laid out with a proper topology [6]. To obtain a full-scale current of ±15 mA, the unity current \( I_U \) was set to 1 mA in both output sections (when a different full-scale current is required, the described topology can be used, adjusting the reference current to a proper value). Thanks to the proposed approach, fairly small transistors could be used to realize the output current sources (the \( n \)-channel transistor which implements the elementary current sink generator has an aspect ratio \( W/L \) equal to 100μm/4μm; the \( p \)-channel transistor which implements the elementary generator of the output current source section is three times larger). Large-signal output resistance requirements were met: computer simulations showed that, with \( V_{DD} = 10 \) V, the variation occurring in the output unity current \( I_U \) due to the output voltage variation is smaller than 8 μA in the range 0.6 V ≤ \( V_{OUT} \) ≤ \( V_{DD} - 0.6 \) V. This allows to obtain the required 8-bit conversion accuracy even when the actuator's resistance is as large as ~300 Ω.

The selection of the currents to be actually delivered to the output in accordance with the digital value to be converted, is obtained by controlling the gate electrodes of the output transistors which implement the binary-weighted output current sources (1, 2, 4, 8 mA). To minimize nonlinearity errors due to mismatching in the currents generated by the sources, these were laid out with a common-centroid topology.

A test chip including four D/A converters together with their control and selection logic was laid out (Fig. 5), and will be integrated by AMS (Austria Mikro Systeme International). Latches are also included in the peripheral of the chip to provide synchronization of the input digital data.
to be converted, thus preventing conversion glitches. The active area of the chip, not including pads and synchronization latches, is 2.25x1.75 mm².

CONCLUSIONS

A system for an efficient digital signal processing and the direct analogue driving of resistive actuators has been proposed. In particular, an application of the proposed technique for the implementation of the display section of a tachometer has been discussed. The described system achieves a significant chip area reduction, while maintaining the required overall conversion characteristics (in particular, accuracy and noise), by using oversampling and linear interpolation techniques. A CMOS D/A converter capable to directly drive a current-controlled actuator has been developed for the presented system. It is characterized by a very large output resistance over a large output voltage range in order to provide a satisfactory linearity even when driving an actuator having a non negligible series resistance. This converter is suited to be integrated in a chip together with the digital signal processing section of the instrument. A D/A converter designed with the described approach can provide an output current of up to few tens mA. When an actuator requiring a larger current has to be driven, a simple bipolar power transistor can be used to obtain the necessary current gain. When a mixed bipolar-CMOS (BiCMOS) technology is available, the bipolar transistor can be integrated together with the converter, thus achieving an optimal integration level.

The analogue section of the system has been designed as a full-custom chip using a conventional 3-μm CMOS technology. The availability of the chip will allow to realize a breadboard for the experimental evaluation of the presented tachometer. The designed digital section, which has also been developed for a CMOS technology, will be implemented on the breadboard with a programmable gate array approach, so the necessary optimization and customization of the system will be carried out.
ACKNOWLEDGEMENTS

This work has been partially supported by the Italian National Research Council (C.N.R.), within the "Progetto Finalizzato Trasporti".

REFERENCES


